COROMETRICS PHASE I REPORT

NEONATAL MONITOR DESIGN

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SUBMITTED TO: DR. TIBOR FOLDVARI

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Dr. Tibor Foldvari   21 November 1980
Corometrics Medical Systems, Inc.
Phase I Report – Neonatal Monitor Design

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1.0   INTRODUCTION

This report is the culmination of Phase I of our contract with Corometrics to provide a full and detailed conceptual design for a portable neonatal monitor capable of performing to the specifications attached in Appendices A & B. We have performed a thorough review of existing neonatal monitor designs and have considered alternative architectures and design approaches for the proposed monitor. This report details the above research, including advantages and disadvantages of the alternatives and our reasons for selecting specific approaches and design implementations. Also provided is a complete set of specifications, including electrical, performance, safety and environmental.

The final section of this report (Section 6.0) is a full and detailed proposal for Phase II of this project to design, build and test a prototype monitor. The proposal details the scope, allocation of responsibility between Octek and Corometrics and the cost and duration of Phase II.

2.0   PRODUCT DEFINITION AND SPECIFICATIONS

The 505/506 neonatal monitors have been well defined by
Corometrics, both in terms of functional and performance
characteristics. These specifications were supplied to
Octek on the 24th of September and updated via a letter
from Patrick Phillips dated October 10, 1980. A copy of
the functional characteristics with the updates is attached
as Appendix A. The updated performance characteristics
are attached as Appendix B. Together they represent the
total design specifications for the engineering model to
be developed in Phase II.

3.0 PRODUCT DESIGN ARCHITECTURE

3.1 Discussion of the Functional Block Diagram

This section describes the function and architecture of the 505/506 monitor at the level of detail shown in the block diagram of Figure 3.1A. The discussion that follows will focus on the definition of the signal processing task of each stage with attention to key system factors that effect the performance of the design. The details concerning particular circuit implementations and technologies are presented in Section 4.

For the purpose of discussion the monitor has been partitioned into five major sub-sections: front end circuitry, physiological processing, display control, CRT drive, and power supply. This division does not necessarily correspond to the physical partition of circuits on the printed circuit cards.

3.11 ECG Front End

The ECG front end consists primarily of a differential amplifier. Only single connection ECG is used with neonates, therefore there is no need for low-level switching of the signals from the patient electrodes.

The ECG differential amplifier must have a common mode rejection ratio (CMRR) greater than 100dB at 60Hz while accommodating up to 5000 ohms source impedance imbalance. Typically, this is achieved by using a third patient electrode connected either directly to the ECG amplifier ground or to a ground-drive circuit. For the 505/506 we plan to implement a two lead ECG system, using a novel ground-drive technique to attain a high CMRR. There is a potential problem with patent infringement (patent #4,200,109), although Corometrics suggested a simplification to the patented two-lead scheme which should get around the patent claims. The two lead ECG is considered a significant advantage for neonatal monitoring.

An important characteristic of the ECG front end which must be dealt with carefully is the ability to survive defibrillator and electrosurgery overloads. The overload problem may be aggravated under battery operation because the overload energy can not be shunted to earth ground. The ECG gain, noise, and input impedance requirements impose no unusual design problems.

3.112 Respiration

The respiration signal will be detected by impedance pneumography, a technique particularly approprate for neonatal monitoring. Impedance pneumograph operates by measuring the patients' impedance to a high frequency signal applied via the ECG electrodes, thus requiring no additional patient connections.

The impedance change during a normal breath is on the order of 1 part per thousand; impedance changes of 1/10 this level should still be detectable. However, to attain this, the high frequency carrier generated in the front end must be extremely well regulated in amplitude, and since the combined patient and lead impedance is somewhat reactive, in frequency.

We plan to demodulate and ac couple the respiration signal in the front end. This will eliminate the problem of sending the full dynamic range of the respiration carrier across the isolation barrier. However, this will require slightly increased circuitry and, since the leads-off signal is not present in the demodulated signal, some means must be provided to separately couple this signal across the barrier.

3.113 Blood Pressure

Blood pressure is detected through a catheter, using a strain-gage type transducer. Power is applied to the transducer (either dc voltage, or possibly pulsed dc to save power), and an output voltage proportional to pressure is generated. The pressure front end ampllfiiers must have stable gain, low noise, and, assuming a dc drive signal, a stable dc offset. The front end generates only a single pressure output, the physiological processing section derives the mean, systolic, and diastolic values from this one signal.

3.114 Temperature

Patient temperatures are monitored by thermistor transducers. The thermistor has a dc resistance that varies nonlinearly with temperature, although well controlled and monotonic.

The temperature front end applies a small signal to the thermistor generating a voltage that is dependent on temperature. The signal is then linearized and amplified, using analog circuitry. The bridge voltage to the thermistor must be below that which would cause more than 0.02o of self heating. This means that the signal level to be processed by the front end amplifier/linearizer will be small; the drift and noise characteristics of the electronics must be carefully controlled.

3.115 Isolation Barrier

All patient electrical connections must be isolated from ground through a very high impedance in order to protect the patient from hazardous electrical currents. To provide this protection, both the power and signals for the front end will be separated from the rest of the instrument by a high impedance barrier. The performance of this impedance barrier or isolation circuit is critical because it affects the signal quality available to all of the following stages. Five separate signals must be passed across the barrier, without introducing significant gain error, offset, or noise. Efficient use of the coupling devices is important, since these are high-cost items.

Both magnetic coupling (transformer) and optical coupling will be considered. A time multiplexing scheme will probably be used to pass all five signals across one isolation device.

Power for the front end will be provided through a small transformer. It will not be possible to use the same transformer for both power and signals, because this technique is covered by patent claims (Patent # 3,988,690).

3.12 Physiological Processing

The physiological processing section accepts the signals from the front end, and generates the signals for the waveform display, the numeric data, the rear panel system connector, and derived parameters as well as the alarm and calibration signals.

3.121 ECG

The ECG waveform processing section conditions the ECG signal for display on the screen, and for output to the rear panel system connector. This conditioning consists of removing the dc component, manual gain control and filtering. The ECG signal has a slowly varying dc component which would move the trace up and down on the screen if not removed. Because the dc reject filter has a long time constant, large dc overloads, as could be produced by defibrillation pulses, could keep the waveform off-screen for several seconds. A fast restore circuit will therefore be added to handle overloads and restore the dc level within 0.5 to 2.0 seconds.

The ECG gain will be set manually; the amplitude of the displayed ECG waveform will be controlled by the position of a front panel potentiometer.

Low pass filtering completes the conditioning of the ECG signal.

The specifications call for a high frequency cut-off of 50Hz. The 50Hz low-pass filter also serves as the anti-aliasing filter for the waveform digitizer. A three pole filter which will have 30dB attenuation at 120Hz should meet this requirement.

Another less severe low-pass filter will be required to condition the signal for output on the rear panel system connector. The specifications call for a high frequency cut off of 100Hz for the system connector output.

3.122 Cardiotachometers

The cardiotachometer circuit derives the instantaneous
and average heart rate from the ECG signal. To accurately
determine heart rate, the circuit must reliably detect the
occurrence of a QRS complex in the ECG signal, indepen -
dently of the ECG gain setting. The detector must recog-
nize only the QRS complex, and reject noise and other ECG
components, including pace pulses.

The beat-to-beat cardiotachometer circuit measures the time
between pairs of pulses from the QRS detector. The inverse
of this time is the instantaneous or beat-to-beat heart rate,
and is used only for the heart rate trend display. The
average heart rate is calculated by averaging the output of
the beat-to-beat circuit over a specified period to time.
The ECG alarm is triggered if the average heart rate goes
outside of the limits set by the front panel controls.

3.123 Respiration Waveform

The respiration signal comes from the front end demodulated
and with the dc component removed. The gain for the respir-
ation waveform will be controlled by a front panel potentiom-
eter; the specifications call for no AGC mode. Before being
applied to the waveform display circuitry, the respiration
signal is low-pass filtered to remove any high frequency arti-
fact and to prevent aliasing.

3.124 Respiration Rate and Apnea Alarm

The respiration breath detector is probably the single most
challenging design in the instrument. This circuit must
accept the highly unpredictable respiration signal and
determine the occurence of individual breaths. If the auto-
matic threshold mode is selected, the detection of breaths
must be independent of the amplitude of the respiration signal.
The automatic threshold tracking circuit will have to be
carefully designed so that artifacts are not mistaken for
actual breaths. The circuit must discriminate between a valid
breath signal, at low amplitude, and artifacts from cardiac
activity, body movements, electrical noise and other sources.
If the breath detector does not reliably reject these inter-
ference signals, apnea can not be reliably be detected.

Special circuitry will be needed to prevent cardiac artifact

from being detected as breathing. The QRS pulse from the
cardiotachometer will be used to lock out the detection
of breaths in synchrony with the heart beat. This is a
challenging task, as the time delay between the QRS,
representing the electrical activity of the heart, and the
heart artifact in the respiration signal, caused by the
mechanical motion of the heart, is not exactly known.

Once the detector has generated a pulse corresponding to
a breath, the breath rate can be determined. This will
be accomplished in a circuit similar to an averaging
cardiotachometer. The breathing rate signal is then sent
to the numeric display section, and to the high breath
rate alarm detector. The apnea detector uses the same
pulse output from the breath detector; if no breaths are
detected after a fixed interval of time, the apnea alarm
is triggered.

3.125 Blood Pressure

The blood pressure processing circuitry provides waveform
information to the display and to the system connector.
In addition, three derived parameters are calculated for
display: mean, diastolic and systolic pressure. The
signal processing is different from ECG and respiration
in that it is dc coupled throughout the instrument.

The first stage of pressure processing is the dc to 40Hz
band limiting filter which eliminates high frequency noise.
This is followed by the auto-zero function. Upon venting
the pressure transducer to the atmosphere and activating
the auto-zero control, the circuit will automatically null
any transducer or electronic offsets, forcing the pressure
reading to zero. The required nulling signal is held
electronically until the next activation of the zero control.
The gain control stage sets the pressure full scale range
in accordance with the two position front panel control.
The systolic, diastolic, and mean pressures are calculated
from the pressure waveform. These three derived parameters
are then ready for numeric display. The diastolic pressure
signal is also used to detect unreasonably high pressures
that may result from improper use of the transducer or asso-
ciated equipment. The pressure alarm circuit, with a fixed
threshold of approximately +300mmHg detects this condition.

3.126 Temperature

Temperature processing consists of adding a dc offset signal
to the signals from the front end, and of low-pass filters
to eliminate noise. The two temperature voltages are then
applied to the numeric display circuitry, and to the system
connector.

3.127 Alarms

The alarm circuitry controls the alarm LED and the audible
alarm 'beeper'. The alarm sounds whenever an alarm condi-
tion exists on any of the following detectors:

    ECG Rate
    Apnea
    High Respiration
    High Pressure

The audible alarm can be disabled via a front panel button,
and its loudness can be controlled by a rear panel poten-
tiometer. In addition, a QRS beep is provided.

3.13 Display Control

The display control section provides for non-fade display of two physiological waveforms, and the numeric display of five parameters. These two functions are for the most part independent, except for some shared timing circuitry.

3.131 Waveform Display

The moving trace, non-fade display format requires that the waveform be repetitively scanned at a rate of 60Hz to prevent any perceived flicker. This will be accomplished by storing the digitized samples of waveform amplitude in a memory circuit which can hold one full screen of data. The memory's read cycle timing requires output of 960 points in 4ms. This is easily handled with standard memory chips. The A/D and D/A converters for the waveform memory will have 8 bit accuracy. The D/A speed must be greater than the data rate to the CRT (4 usec/sample). The A/D conversion rate, however, is slow, since it needs to convert at the waveform sample rate of 240 samples/sec/waveform. A single A/D converter will serve both waveforms.

To achieve the moving trace format, the memory control circuit causes the display of all data in the memory to periodically advance to the left by one screen position. This will be done synchronously with the writing of new data from the A/D converter.

Front panel controls will select the trend mode, where the moving trace is slowed by a factor of fifty. A "Freeze" mode will also be provided in which the traces do not move and are not updated.

3.132 Parameter Display

The parameter display section accepts the analog signals from the physiological processing circuits and displays these in decimal form on the CRT. This section consists of an A/D converter, a memory, and a character generator. A single BCD A/D converter will be used for all parameters. The converter will have three digit accuracy. The speed requirements for this A/D can be easily met, since each parameter needs to be converted only once every two seconds.

As the A/D converts, the parameter memory stores each resultant digit as a separate character. As the numeric values are displayed, each character is read in its turn from the memory. The character generator decodes the character

code, and drives the CRT X,Y, and Z amplifiers to trace
out the correct digit.

3.14 CRT Drive

The CRT drive circuitry consists of amplifiers, power
supplies, and controls necessary to control the CRT
beam. Horizontal (X), and vertical (Y) deflection
amplifiers boost the X and Y control signals to the
appropriate voltage levels. A video (Z) amplifier con-
trols the beam intensity and blanking. Bias voltages
for the anode and grids are generated by the high volt-
age power supply. Controls for focus, intensity, and
astigmatism will be provided.

3.15 Battery/AC Power

The monitor will be operated either from an internal
battery or from ac power. Whenever the unit is plugged
into an ac outlet, the battery will be charged at an
appropriate trickle rate, and power to operate the in-
strument will be taken from the ac line. A 'battery
low' LED will indicate when the battery voltage has
dropped below a preset level.

3.2 DESIGN GUIDELINE DISCUSSION

The design considerations of the 505/506 neonatal monitors covered in this report are primarily based on the specifications of the 503/504 monitors. The essential product goals and design guidelines followed in assessing the circuit implementation for these monitors are based on three major concepts:

1) Maintain the positive features of the 503/504,
2) Improve the undesirable features, and
3) Add features and capabilities to improve performance and marketability.

Some of the attributes of the 503/504 that will be maintained include:

1) Light weight,
2) Small package,
3) Low power dissipation (long battery life), and
4) Low cost.

Some of the undesirable features that will be improved upon include:

1) Poor reliability
2) Poor serviceability,
3) Appearance, and
4) Operator interaction

There are seven specific additions that will provide improved performance and marketability:

1) Two temperature inputs and display,
2) Heart rate trend display,
3) Pressure auto-zero,
4) Two lead ECG,
5) Automatic gain control (AGC) on ECG,
6) Tracking (Auto) threshold on respiration, and
7) Improved apnea alarm

Having reviewed the specifications and design of the 503/504 and the requirements for the 505/506, we feel confident in being able to meet these design goals to your satisfaction. We have some concern about the size and power dissipation. This is because the added features may increase the size somewhat, and, although we have found several areas in which we can conserve power, it may be difficult to keep the

total dissipation under 4.5 watts. The only other areas
of major concern are the two-lead ECG circuit (which is
mainly a patent issue to be assessed by your legal staff),
and the effectiveness of the tracking threshold on the
respiration signal. These areas of concern only indicate
where additional effort will have to be placed to attain
an acceptable design rather than real compromise in the
design goals.

3.21 Power

The 505/506 monitors are designed to be portable. In
order to meet the requirements of relatively low weight
and reasonable battery life, the 505/506 will use the
same or equivalent battery as the 503/504, and the power
dissipation will be held to be approximately 4.5 watts.
Since the new design will include additional power con-
suming circuits, this will not be easy. However, there
are a number of areas in which improved circuit design
can significantly lower the power dissipation. These
include:

1) Use of a lower pressure transducer voltage.
2) Pulsing the pressure transducer voltage.
3) Use low power op-amp and comparators (this
   alone can save approximately 0.75 watts.)
4) Use a 16K dynamic RAM instead of shift regis-
   ters.
5) Use one switching power supply instead of three.
6) Use a lower anode voltage CRT. (This will
   result in a slight brightness penalty, however,
   a neutral density or circular polarized screen
   may regain the lost brightness

3.22 Reliability

Reliability is always an important item in electrical
equipment. It is of particular importance in medical
equipment. Unfortunately the medical equipment environ-
ment can be very harsh, particularly for portable equip-
ment. Besides mechanical abuse, the 505/506 must with-
stand high electrostatic discharges, extreme line trans-
ients and defibrillation pulses. All circuitry, particularly
static sensitive circuits such as CMOS, will be designed with
careful consideraiton given to the electrical environment.

3.23 Size/Volume

The product goal for the mechanical size and volume of the 505/506 is to keep approximately the same size and form factor as the 503/504 monitor. There is also a desire to improve the serviceability of the 503/504 which must be considered when discussing size and volume. Because the 505/506 goals are stated as a function of the 503/504, it will be convenient to compare the new design(505/506) to the 503/504, with possible improvements pointed out.

The mechanical design of the 503/504 has several major deficiencies. For example, the front panel arrangement of controls did not consider operator ease-of-use. By mounting all button controls on the pre-amp circuit board and all potentiometer controls on the heart rate circuit board, the manufacturing cost of the 503/504 was reduced, but at the cost of accessibility, serviceability, safety, and ease-of-use. A significant improvement would be to mount all front panel controls on one printed circuit subassembly so that neither the front panel layout nor the mounting of the remaining circuitry are constrained.

Another deficiency of the 503/504 was the use of one large top-mounted circuit board with no protection from high voltage circuitry. This board must be removed to access any internal components, and causes a safety hazard and decreased reliability. This technique may have saved volume, and improved manufacturability, but at the cost of safety, reliability, and serviceability. Corometrics' mechanical design team has an approach using six closely spaced PC boards. We concur that this will provide the required board space and will not compromise the performance or other aspects of the design. To accommodate this physical layout, and for improved reliability, the 505/506 will be designed with a separate high voltage and power supply assembly. This will remove the large components and the high voltage from the main circuit boards, allowing the boards to be mounted on close centers. In this way, the volume of the 503/504 can be maintained in the 505/506.

3.24 Regulations

The 503/504 is a patient connected medical instrument that will be marketed worldwide and must, therefore, conform to those standards set forth by several worldwide agencies.

These standards include the following:

    V.A. x 1414
    UL 544
    CSA 22.2 #125
    NEMKO
    I.E.C. 601.1
    AAMI "Safe Current Limits"

These standards specify leakage currents, patient impedances,
power transformer requirements, and test procedures. From a
circuit design standpoint, the product specifications de-
tailed in Appendix B cover most of the pertinent standards.
Since Corometrics has extensive experience in this area, Octek
will rely heavily on their expertise for guidance concerning
medical equipment standards.

3.25 Patents

We have reviewed fifteen patents related to medical monitors
that were sent to us by an American Home Products Patent
attorney (Eugene Flanagan). A list of the patent numbers
and a very brief description of each is provided in Appendix C.
There are four specific patents that could handicap our de-
sign. The first is Becton Dickenson's patent (#3,948,250)
on "Physiological Information Display". This patent covers
the 7 segment numeric display generator used in their 503/504
monitor. Although this is a very inexpensive circuit, we
plan on using a more sophisticated display method to gener-
ate more readable numbers and are therefore not concerned with
this patent.

The second patent which could be a problem is Hewlett Packard's
(by Rick McMorrow) "Coupling Circuit with Driven Ground",
patent (#4,200,109) which covers their two-lead ECG implemen-
tation. However, American Home Products patent attorneys
indicate that small changes in the circuit that do not sig-
nificantly affect performance can be made that will circum-
vent the patent claims. We will follow their direction in
the use of this circuit.

The third potentially conflicting patent is one assigned
to Becton-Dickinson and entitled "Physiological Monitoring
System" (#3,587,567). This patent covers the use of the
switching power supply oscillator as the source signal for
the impedance pneumograph circuit. We will have to work with
American Home Products attornies concerning our design since

we plan on using a similar circuit. However, there are
several differences, including significant improvements
by using the same signal for multiplexing the signals
over the isolation barrier.

The fourth patent (#3,988,690) is entitled "Amplifier
Circuit Having a Floating Input Stage". This circuit
uses a single transformer to couple both signal and
ac power to the isolated front end. Although potentially
useful in the 505/506 design, there is not a great savings
in this approach. Also there are several alternative
design approaches.

3.3   Major Architectural and Design Decisions

Certain overall design decisions must be made prior to any
specific circuit design. We have isolated specific design
alternatives that have a major impact on overall performance
and cost, and have researched these alternatives to determine
the optimum approach to meet the design goals. A brief sum-
mary of the alternatives considered and our decisions follows:

1) Use a microprocessor, or conventional analog/digital
   hardware for processing of the derived parameters and
   other functions.
   The microprocessor approach will be considerably more
   expensive and will not provide appreciable benefits,
   and is therefore not recommended.

2) What method will be used for the patient isolation
   barrier?
   All isolated signals will be preamplified on the floating
   side and multiplexed onto a single isolation transformer.

3) What will be the design approach used for the bright wave-
   form display?
   We recommend using a 16K bit dynamic RAM for the moving
   trace waveform display.

4) What type of display format will be used for the CRT num-
   erics?
   A stroke graphic technique has been selected as superior
   because it generates significantly more attractive and
   readable characters than does a seven-segment or dot
   matrix approach. However, there is a cost penalty.

5) What is the optimum approach for the system power
   supplies?
   Our study suggests the use of one switching power supply
   to supply all voltage: plus and minus ten volts (for
   linear circuitry and CMOS), plus five volts for TTL and
   NMOS, and all CRT voltages.

6) Which circuit families for analog circuitry and logic
   circuitry are preferred for this design?
   Most of the circuits will be implemented in low power
   programmable op-amps, low power comparators, and CMOS
   switches. Digital circuitry will be implemented in CMOS
   where possible, LSTTL elsewhere.

3.31 Microprocessor Analysis

One of the most significant decisions involving the design
of the 505/506 monitor concerns implementing some or all the
traditional hardware circuitry with a microprocessor. With
the present low cost and extreme versatility of today's
microprocessors it is often cost effective to replace dig-
ital logic and analog circuits with a microprocessor. We
have methodically reviewed all aspects and functions of the
505/506, evaluated each function for potential microprocessor
implementation and then compared the cost, board space
and power requirements for those functions that could be
performed with a microprocessor. The results do not favor
a microprocessor implementation.

The required board area, cost, and power to implement each
function in analog and digital hardware can be estimated
based on the amount of circuitry that is required. Estimating
the cost of the microprocessor approach is more complicated.
A certain hardware and software cost is associated with
simply using a microprocessor, independent of the number of
functions is is performing. This overhead consists of the
microprocessor, its associated clocking, decoding, control,
and buffering hardware, and some overhead firmware.

Each function that the microprocessor performs requires some
input or output (I/O) hardware in order to operate; the cost
of this hardware was estimated on a function by function basis.
The amount of RAM and ROM required was estimated for the en-
tire system as a function of the number of tasks that are to
be implemented. When board area, pricing, and power for all
individual functions have been estimated, totals for different
subsets of the total number of functions can be estimated
and compared, hardware versus firmware.

3.32 Firmware Versus Hardware

Some of the functions of the 505/506 are not appropriate for
implementation in microprocessor firmware because of high
speed requirements, low signal levels or other obvious rea-
sons. These functions include the following:

Front end circuitry: Requires low noise linear amplifica-
                       tions.

Display Circuitry: Requires real time high speed control
                       of CRT beam; CMOS is best suited.

Power supply cir-
cuitry: Dedicated circuitry is required.
CRT drive circuitry: Requires high voltage linear ampli-
                       fication.

Most of the functions that are involved with physiological processing are appropriate tasks for a microprocessor. These functions have high level analog input signals with low bandwidth requirements; all provide low rate output data such as digital readouts, LED control, slowly varying analog voltages, alarm control etc. These requirements are compatible with microprocessing speeds. Below is a list of physiological processing functions and our appraisal of whether each is appropriate for microprocessor implementation.

1. ECG dc level restore.
    Not appropriate because of the wide dynamic range required.

2. ECG AGC.
    Not appropriate because of the wide dynamic range required.

3. ECG display - 50Hz filter.
    Not appropriate since anti-aliasing filter is required
    prior to digitization anyway.

4. ECG pace pulse reject.
    Probably a good function for a microprocessor.

5. ECG QRS filter.
    Appropriate function.

6. QRS detect.
    Appropriate function.

7. Beat-to-Beat cardiotach.
    Good microprocessor task involving low rate period measure-
    ment.

8. Averaging cardiotach.
    Good microprocessor task.

9. Alarm functions.
    Good microprocessor task; slow logical decisions.

10. Calibration signal.
    Should be done as early as possible in analog circuitry;
    Not appropriate.

11. Respiration dc level restore
    Not appropriate due to wide dynamic range required.

12. Respiration filtering.
     Requires some anti-aliasing filter, but much of the
     filtering could be performed in firmware.

13. QRS artifact reject.
     Good application for digital signal processing.

14. Breath detect.
     Good application.

15. Apnea alarm and high respiration alarm.
     Good application.

16. Respiration rate meter.
     Good application.

17. Blood pressure auto-zero.
     Should be done prior to digitizing since it affects
     dynamic range by 2:1; not appropriate.

18. Gain control for waveform display.
     Should be done prior to digitizing since it affects
     dynamic range by 5:1; not appropriate.

19. Pressure parameters: mean, systolic, diastolic.
     Good application for microprocessor.

20. Excess pressure alarm.
     Good application.

21. General alarm logic.
     Good application.

22. Numeric display formatting.
     Good application since derived parameters would be
     determined by processor. Display refresh buffer could
     be filled by the processor.

23. Waveform digitization and display memory data entering.
     Good application since waveform must be digitized prior
     to any microprocessor functions.

24. Control panel.
     Good application since processor must read position of
     switches in order to change modes.

Of the above appropriate functions, we feel that the following
are the least risky and the most likely to provide significant
cost savings over a hardware approach.

1) Waveform digitization and display memory data entry.
2) Parameter digitization.
3) ECG pace pulse reject.
4) ECG QRS filter.
5) ECG beat detect.
6) Beat-to-Beat cardiotach.
7) Averaging cardiotach.
8) All alarms.
9) Pressure parameters (except gain and auto-zero).
10) Respiration parameters (except gain and dc level restore).
11) Display formatting.
12) Control panel.

Since it is not good design practice to switch back and forth
between digital and analog processing, we will assume that
the digitization stage will immediately follow the gain,
offset, and filter stages and that all subsequent stages
will be all digital up to the display hardware.

The proposed microprocessor hardware design is composed of
the following: A general purpose microprocessor, RAM for
variables and state storage, ROM for program and constant
data storage, I/O (to digitize analog signals, read the
front panel controls, interface to the display hardware,
and provide status indicators), and a parallel 8x8 multi-
ply/divide unit to improve processing speed.

The microprocessor considered most appropriate for this
application is the RCA, 1802 8-bit CMOS processor. A typical
NMOS processor would be less expensive ($5.00 compared to
$10.00 for the 1802), but would consume almost 0.5 watts
compared to 5mW for the 1802. Because 0.5 watts is a sig-
nificant power draw, the power savings associated with the
1802 justifies the additional cost. Another CMOS candidate
is the slightly more expensive 12-bit Intersil 6100 micro-
processor. The support circuitry for the processor consis-
ting of clock circuitry, buffering, and memory and I/O de-
coding which will also be implemented in CMOS to conserve
power.

CMOS RAM and CMOS ROM will be used. We estimate that 256
bytes of RAM and 4K bytes of ROM will be required to im-
plement all of the above processing functions. I/O, also
CMOS, will be added into the pricing tables on a function-
by-function basis. The CMOS 8x8 multiply/divide unit (RCA
CD1855) will increase the digital signal processing speed
of the processor by a factor of 100; this speed increase is
mostly a function of the processor's increased ability to
perform high speed multiplications. Without it, none of
the ECG and pressure functions could be implemented, except
for the cardiotach circuitry, which is relatively slow.

The guidelines that were used to determine price, power dissipation, and PC board area for circuit implementations are listed in Table 1. (Page 3.3-9).Factory costs assume 100 units per year and includes board loading. Table 2 indicates the I/O hardware required to implement the various microprocessor firmware routines. The functions that do not require I/O are in the middle of the processing stream (digital data in from another function, digital data out to a different function). Table 3 indicates the estimated cost, power and board area for the hardware that is necessary to implement each function without a micro-processor (using discrete analog and digital circuitry). Table 4 indicates the cost of the microprocessor overhead, with and without a CMOS 8x8 multiplier.

Based on the information tabulated in tables 1-4, the hard-ware necessary to implement all functions was totalled and comparisons of hardware versus firmware were made. The microprocessor hardware costs were based on several assump-tions. It was assumed that the ROM required for the program to implement all of the functions would be 4K bytes and that the RAM required for variable, data, and machine state. storage would be 256 bytes. Also, since several of the functions require digital filtering and digital signal processing the 8x8 multiplier will be required to handle these tasks in the time available. The total requirements for the microprocessor based system (called System A) are listed in Table 5. The total requirements for the discrete circuitry approach (called System B) are listed in Table 6. The estimated costs, power dissipations, and board areas for Systems A and B are compared below:

	System A (Microprocessor)	System B (discrete circuitry)
Cost	$103.00	$54.90
Power	109mW	190mW
Board Area	47.5 sq. in.	46 sq. in.

The microprocessor approach (A) will cost nearly twice as much, require approximately the same board real estate, and save only 81mW of power over over the analog approach (B). The small power savings is obviously not worth the cost. This is particularly true considering the added risk of using a microprocessor and the potentially longer development time.
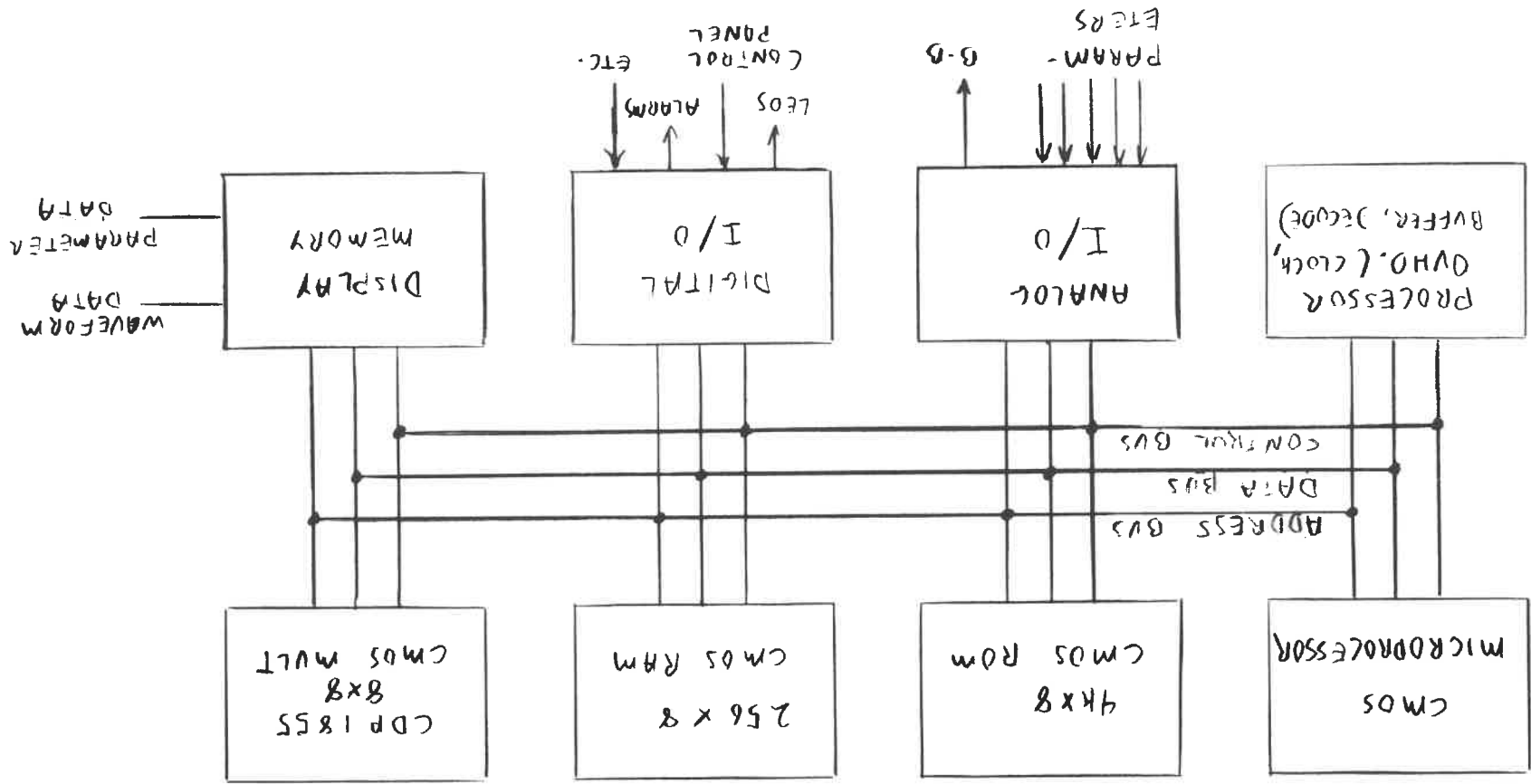
A second pair of systems was considered since it is possible that savings could be realized by using less microprocessor capability. System C is designed to perform only the low speed processing tasks listed in Table 7. The multiplier has been eliminated, the ROM reduced to 1K bytes, and the RAM reduced to 128 bytes. System C is compared to system D, (Table 8) the discrete circuitry approach to the same functions, below:

	System C (Microprocessor)	System D (discrete circuitry)
Cost	$55.00	$38.50
Power	49mW	125mW
Board Area	39 sq. in.	32 sq. in.

For this system also, the microprocessor approach costs more (nearly $20.00 extra), saves only 75mW, but would use 7 square inches of additional board space. From a cost point of view, the microprocessor approach is not a good choice for either pair of systems.

Other factors that might make the microprocessor approach more favorable were also considered. These include product flexibility, factory and field serviceability, product development cost and time, and project risk. Of these, only product flexibility will benefit substantially from a micro- processor. By implementing functions in microprocessor firmware, changes and additional features can be added at minimal development and manufacturing cost. This product is aimed at the low end of the market, and its functions are well defined. Therefore, this is not considered to be an advantage. Besides, the addition of parameters such as blood gas or cardiac output measurement would require sub- stantial front end circuitry, forcing a considerable rede- sign anyway.

Of the other considerations, factory and field serviceability have both advantages and disadvantages. Typically in a microprocessor based design, if one component fails, the processor is prevented from performing any tasks making the entire unit inoperative. However, the number of com- ponents is less, which results in an improved reliability and ease in trouble-shooting. In an analog hardware approach, when a pressure circuit component fails, for example, it is likely to only affect the performance of the pressure cir- cuitry.

Product development cost and time, and project risk are increased substantially by the use of a microprocessor. The development time for the microprocessor hardware would compare roughly to the development time for the analog hardware necessary to implement the functions. The microprocessor firmware would require additional development time. We estimate that this task would add 10% to 20% to the Phase II development time and budget. Since most of the functions have previously been implemented in hardware by Corometrics, Octek staff, or other companies, there is little relative risk involved in this approach. However, the firmware approach is new, and represents several unknowns (such as quantization error, microprocessor time constraints, etc.). The relative risk is therefore higher.

After examining all these considerations, it appears that the only gains that are realized by microprocessor implementation are in flexibility (considered unimportant in this product) and insignificantly lower power dissipation (approximately 2% of the total product). Losses would be incurred in factory cost, development cost and time, and risk. Board real estate and serviceability would be equivalant. Our recommendation is therefore to implement the processing functions with analog and digital circuitry, and to avoid the use of a microprocessor for this project.

Qty.

Qty.

	Factory Cost $	Power mW	Area Sq. In.
1 Low Power op-amp	.50	7.0	0.5
1 Comparator (LM 339)	.20	1.0	0.5
1 Byte ROM, CMOS (Part of 1K, $10)	.015	0.01	0.002
1 Byte RAM, CMOS (Part of 1K, $10)	.04	0.04	0.01
1 Resistor, 1%	.10	–	0.1
1 Capacitor, typical	.20	–	0.1
1 Diode, signal	.10	–	0.1
1 CMOS IC	.50	–	1.0
1 CMOS switch	.25	–	0.5
1 Input or output port, 8 BIT, CMOS includes decoding	2.50	1.0	1.5
1 Analog out, S/H type (1SW, 1 op-amp, 1 cap, 1/8 I/O port, One D/A used for all analog I/O functions)	2.00	10.0	1.0

TABLE 1

Pricing Estimates of Individual Components

Function	Hardware Notes	Cost $	Power mW	Area Sq.In.
B-B cardiotach	Uses waveform data Outputs: analog signal	2.00	10	1
Averaging cardiotach	None	0	0	0
Beat detect	None	0	0	0
QRS Filter	None	0	0	0
Pace pulse reject	None	0	0	0
Alarms	Digital I/O to Read Pots.	3.50	3	4
Waveform digitization	Same as non/micro	11.50	10	7
Parameter digitization	Uses part of waveform	2.00	10	1
Display formatting	I/O to load display buffer	3.00	5	5
Pressure parameters	None	0	0	0
Respiration parameters	None	0	0	0
Control panel	I/O Ports; digital	2.50	1	1

TABLE 2

Microprocessor I/O Hardware Required

Function	Notes	Cost $	Power mW	Area Sq.In.
B-B cardiotach	3 op-amp/comparator	1.50		
	1 switch	.50		
	15 discretes	2.00		
	Totals	4.00	25	3
Averaging cardiotach	20 op-amp	1.00		
	One shot	1.00		
	15 discretes	1.50		
	Totals	3.50	25	3
Beat detection	1 comparator	.20		
	10 discretes	1.50		
	Totals	1.70	10	2
QRS filter	1 op-amp	.50		
	10 discretes	1.50		
	Totals	2.00	10	2
Pace pulse reject	1 op-amp	.50		
	8 discretes	1.20		
	Totals	1.70	10	2
Alarms	5 comparator	1.00		
	20 resistors	2.00		
	Logic	.50		
	Totals	3.50	10	4
Waveform digitization	1 D/A (8 bit)	4.00		
	1 op-amp	.50		
	10 resistors	1.00		
	1 SAR	3.00		
	1 MUX	1.00		
	Control logic	2.00		
	Totals	11.50	10	7
Parameter digitization	1 Dual slope A/D, BCD	5.00		
	Logic	2.00		
	Totals	7.00	10	4

TABLE 3
(continued on next page)
Analog Circuitry Required

Function	Notes	Cost $	Power mW	Area Sq.In.
Display formatting	Control logic	3.00		
	Totals	3.00		5
Pressure parameters	5 op-amps	2.50		
	2 analog switches	1.00		
	20 discretes	3.00		
	Totals	6.50	30	5
Respiration	6 op-amps	3.00		
	4 analog switches	1.00		
	30 discretes	4.50		
	Control logic	2.00		
	Totals	10.50	40	8
Control panel	Control logic	2.00		
	Totals	2.00	10	3

TABLE 3

Analog Circuitry Required

	Cost $	Power mW	Area Sq.In.
Processor, RCA 1802	10.00	5	4
Support IC's (clock, decoders, buffers)	8.00	10	10
Totals	18.00	15	14
Multiplier, 8 x 8	20.00	5	4
Total w/multiplier	38.00	20	18

TABLE 4

Microprocessor Overhead

SYSTEM A

All functions implemented in firmware.

Assumes: 4K CMOS , 256 bytes CMOS RAM, 8x8 multiplier.

	Cost $	Power mW	Area Sq. In.
256x8 RAM	10.00	10	2.5
4Kx8 ROM	40.00	**40**	8
Processor Hardware	38.00	20	18
B-B cardio I/O	2.00	10	1
Averaging cardio	0	0	0
Beat detect	0	0	0
QRS Filter	0	0	0
Pace pulse reject	0	0	0
Alarms	3.50	3	4
Waveform digitization	2.00	**10**	7
Param. digitization	2.00	10	1
Display formatting	3.00	5	5
Pressure parameters	0	0	0
Respiration parameters	0	0	0
Control panel	2.50	1	1
Total	$103.00	109mW	47.5 Sq. In.

TABLE 5

System Pricing : all functions done in firmware

SYSTEM B

All functions implemented in hardware.

	Cost $	Power mW	Area Sq. In.
B-B cardiotach	4.00	25	3
Averaging cardiotach	2.00	25	2
Beat detect	1.70	5	1.5
QRS filter	2.00	10	1.5
Pace pulse reject	1.70	10	**2**
Alarms	3.50	10	4
Waveform digitizing	11.50	10	7
Parameter digitizing	7.00	10	4
Display formatting	3.00	5	5
Pressure parameters	6.00	30	5
Respiration parameters	10.50	40	8
Control panel	2.00	10	3
Total	$54.90	190mW	46 Sq. In.

TABLE 6

System Pricing: all functions in hardware

SYSTEM C

Slow Functions implemented in firmware,

	Cost $	Power mW	Area Sq. In.
128 x 8 RAM	5.00	5	5
1K x 8 ROM	10.00	10	2
Processor hardware	18.00	15	14
B-B cardiotach	2.00	0	1
Averaging cardiotach	0	0	0
Alarms	3.50	3	4
Waveform digitize	11.50	10	7
Display Formatting	3.00	5	5
Respiration parameter	0	0	0
Control panel	2.50	1	1
Total	$55.50	49mW	39 Sq. In.

TABLE 7

System Pricing : low functions done in firmware

SYSTEM D

Slow Functions implemented in hardware.

	Cost $	Power mW	Area Sq. In.
B-B cardiotach	4.00	25	3
Averaging cardiotach	**3.5**0	25	2
Alarms	**3.**50	10	4
Waveform digitizing	11.50	10	7
Display formatting	3.00	5	5
Respiration param.	10.50	40	8
Control panel	2.00	10	3
Total	$38.50	125mW	32 Sq. In.

TABLE 8

System Pricing : slow functions done in hardware

3.33   Isolation Method

For safety reasons, electronic equipment that is connected
to a patient must provide a high impedance to the hospital
electrical ground.   The best way to implement this with
today's technology is to isolate the circuitry that connects
to the patient from ground, passing the signals through a
medium that does not pass high common mode voltages.   The
two methods that will be considered for this isolation
barrier are the transmission of light energy via opto-
couplers, and the transmission of magnetic energy via
transformers.

The electronics for either method can be expensive both
in parts cost and board real estate.   Time multiplexing
of the five signals that must be passed from the isolated
side to the grounded side could substantially reduce the
cost and board area.   Although no other neonatal monitors
use this technique, we feel it is a viable approach and
we will thoroughly examine this approach in Phase II.
There are several potential schemes to synchronize the
grounded and isolated sides.   Since a high frequency power
transformer is required to transmit power to the front
end, the transformer frequency can be used as the multi-
plexing clock.

3.34   Waveform Display

The product specifications call for the display of two
analog waveforms with an analog sampling rate of 240Hz.,
and with four seconds of data display.   Eight bits of vol-
tage quantization are needed for each waveform.   Therefore,
the memory required is 8x2x240x4; to the nearest power of
2, 16,384 bits are required.   In light of the low power
requirement for the instrument, the applicable memory
technologies are:

1)   Dynamic shift registers
2)   Static CMOS RAM
3)   Dynamic NMOS RAM

The use of dynamic shift registers is attractive because
a memory address counter is not required to implement the
moving trace display, also it is relatively easy to create
the 8 bit wordsize for the analog storage.   The disadvantage
of using shift registers results from the fact that the
technology has not advanced significantly over the last

several years, as it has with dynamic RAMS. The result is
a somewhat higher price and power per bit, and higher
package count. Also, since few of these devices are
being designed into new products, their availability may
decrease in the future.

Static CMOS RAM is very attractive from the point of view
of power and word size, but their cost eliminates them for
this application.

Dynamic NMOS RAMS, especially the 16K by 1 bit size, offer
fairly low power, very low cost, and low package count.
Their disadvantages are the relatively complex support
circuitry needed to deal with the one bit organization,
the fairly tight timing constraints when running the de-
vices at near maximum speed, and the need for refresh support
during the time the analog traces are not being displayed.

By using a single supply, low power 16K dynamic RAM (Intel
2118), a significant power savings can be realized over the
shift register implementation, even when the support cir-
cuitry is taken into consideration. A memory system power
of about 150mW can be achieved in this way, compared to
about 490mW for the current 503/504 shift register implem-
entation. The PC area required is about the same.

With the less expensive triple supply 16K RAMS (approximately
$5.50 versus $10.50 for the 2118), about 330mW of power
would be needed. However, the additional power supply would
add cost and board space.

Another possibility is the 2K x 8 dynamic RAM now being made
by Mostek (4816). This device could achieve even lower memory
system power (∼ 75mW) and reduced package count, since it
would require little support circuitry. Unfortunately, the
current price is rather high - $22.00.

At this time, the most attractive alternative is the Mostek
4816 dynamic RAM. Although it's cost is higher, and the
chip count is approximately the same as the 2118 approach,
it does save system power (75mW) and simplify system design
and timing. The part is relatively new, but second sources
are coming on line, and its cost is expected to drop.

3.35 Numerics Display Method

The purpose of the numerics display circuitry is to display heartrate, respiration rate, temperature, and three pressure parameters in clear readable form on the CRT. The inputs to the numerics circuit are well defined analog voltages representing the various parameters. The outputs from the numerics circuit are low level CRT control signals driving the CRT X, Y, and Z channels. The numeric display circuitry is responsible for digitizing the analog voltages at a specified update rate, storing the digitized values into memory, accessing the values at the correct time in the CRT display cycle and controlling the CRT to draw the characters that comprise that digitized value onto the CRT face. Besides character size and contrast, the factor that has the most impact on display legibility and circuitry architecture is the selection of a display method. There are four basic methods of generating characters on a CRT face:

1) The starburst method
2) The Lissajous method
3) The dot matrix method
4) The stroke method

The starburst method consists of a fixed pattern of between 7 and 24 segments (7 for numerics only, 15 to 24 full alpha-numerics) which the deflection circuitry traces for every character. A particular character is stored in memory as one bit per segment and the bit controls whether the segment is visible or blanked for that character. The advantage of the starburst method is its relatively low ROM requirement for the character set, and therefore its relatively lower cost. The disadvantage of the starburst method is the relatively poor character quality, particularly when only 7 segments are used.

The seven segment display used in the 503/504 monitor uses a patented modification of this technique to generate numerics on the CRT. The starburst pattern generates a fixed box-type font and therefore does not allow much flexibility in choosing the character shapes.

The second method is the Lissajous method. This technique was used in very early graphics systems and is now considered outmoded. It consists of Lissajous patterns and parts of Lissajous patterns in the form of strokes, arcs, circles and ellipses, and is best suited to the display of very smooth lower case letters. The control hardware for this scheme is relatively expensive.

The dot matrix method of character display is well suited
for applications where the display medium is organized in
regular lines or a pattern. It is ideal for displaying
characters on a raster scan CRT or on an array of LEDs
or other fixed light sources. For example, many CRT
terminals use this method. Technically, each dot is
represented in a ROM array as one bit of data. As the
CRT beam or the LED selection logic scans by a dot, the
appropriate bit of the ROM corresponding to the desired
character is accessed. If the bit is a "1" then the dot
is displayed. If the bit is a "0" then the dot is blanked.
Standard matrix sizes for dot matrix characters are 7x9
and 5x7 requiring 63 and 35 bits respectively per charac-
ter. This type of character generation is relatively in-
expensive if raster scanning already exists. In conjunc-
iton with a directed beam CRT, additional circuitry and
cost is incurred in generating the raster. The appearance
of the characters is fair for small 5x7 characters, good
for small 7x9 characters and poor for large characters
where the dots are more visible. The size of the char-
acters on the 505/506 CRT would be considered large from
small viewing distances ($<$ 3 feet) and small from large
viewing distances ($>$ 6 feet).

The stroke method is the most general purpose of all
methods. By directing the beam horizontally and vertic-
ally across the CRT face, any character font can be dis-
played. Modern directed beam graphics systems provide
very attractive, highly readable characters of any size
with this method. The amount of ROM required for each
character depends on the accuracy of beam positioning
required and the number or segments per character. At
a maximum of sixteen segments per character and four bit
accuracy required for positioning in both axes, each char-
acter requires 128 bits of ROM. This is approximately
twice the requirement of a 7x9 dot matrix and sixteen
times the requirement of a seven segment display. If the
character set consists of "0" through "9", "-", ".",
" ", there are a total of thirteen characters. For this
character set the seven segment starburst approach requires
104 bits of ROM, the 7x9 dot matrix approach 832 bits of
ROM, and a stroke method 1664 bits of ROM.

Because it is outdated, ill-suited for displaying numerics, and expensive, the Lissajous method will not be considered. Of the other three methods, the stroke is the most physically attractive and readable, dot matrix is next, and starburst (seven segment) is the least attractive. Seven segment starburst characters use the least amount of ROM (typically an off-the-shelf seven segment decoder). Dot matrix characters will require a 1024 bit ROM and stroke characters will require a 2048 bit ROM. The control circuitry for the seven segment method is the least complicated and least expensive. The control circuitry for dot matrix is about 20% more complex, and the stroke control circuitry is about 50% more complex. The cost and complexity of the different methods is therefore proportional to the attractiveness and readability of the characters.

Based on the fact that Corometrics has indicated that improved character readability is very important, we recommend using the stroke generation approach. The numerics display circuit is only a small part of the total monitor and therefore will not significantly increase the total cost. The improvement in the readability of the digits will be significant.

3.36 Power Supplies

There are several general alternatives for the power supply design. The 505/506 monitor will require several different supply voltages at various power levels allowing many possible configurations. The basic choice of power supply technology (linear versus switching) must be determined, as well as the circuit topology. An example of one topology is the power circuitry of the 503/504. It uses one switching step-down regulator to generate a regulated +10 volt supply which drives most of the monitor's logic and linear circuitry. The +10 volt regulated supply is also used as the power source for a multiple output, unregulated, switching supply which provides all of the remaining voltages.

There are two basic problems with this topology. The first is that since the power source for the second supply comes from the output of the first supply, it's efficiency is the product of both supplies efficiencies, which must be lower than if a single supply was used. The second problem, which is probably the reason for the noise on the display, is that the two power supplies are allowed to free run, causing beat frequencies that can interfere with low level and display circuitry. A better approach is to use one switching power supply to generate all of the voltages.

There are two specific parts to the 505/506 power supply circuit. The first part includes the unregulated dc and the battery charging circuit. The unregulated dc circuit provides power for the battery charger and for the monitor circuitry from the ac line when it is available. The battery charger provides a constant current to the battery to provide trickle charging.

The second part of the power supply circuitry takes the unregulated dc or battery voltage and generates all of the power supply voltages for the monitor. The battery operation time is proportional to the efficiency of this power supply. Since switching power supplies have typical efficiencies of 70% to 95% and linear power supplies have typical efficiencies of only 30% to 60%, our choice is a switching supply.

The power supply voltages that are required are a function of the circuit technologies used. For all TTL logic and NMOS memory a +5.0V supply is required. Since most of the logic will be implemented in CMOS, and since CMOS requires a higher power supply voltage for maximum operating speeds (required in some sections), a supply of between +10.0 volts and +15.0 volts will be necessary. The analog circuits, consisting mostly of amps and comparators, will require symmetrical supply voltages of between +5 volts +15 volts. The power draw of these components is proportional to the supply voltage (most internal circuitry operates under constant current) therefore suggesting the use of the lowest supply voltage possible. However, the dynamic range of the op amps is limited by the supply voltages. To maximize the dynamic range, we would use the higher supply voltages. The resolution of this conflict requires a compromise; we recommend using ±10 volts as a good compromise. By operating the CMOS and the linear circuitry from a common supply (+10.0 volts) the necessary connections between analog and digital circuitry are simplified.

High voltages are required for the various functions of the CRT. Voltages on the order of +75 volts to +200 volts are required for the deflection amplifiers; +2000 volts to +4000 volts is required for the second anode of the CRT. Generally, this voltage is tapped via high resistance voltage dividers to supply all of the various CRT grids. 6.3 volts is required for the heater of the CRT.

To summarize, starting with an unregulated source of dc power (battery or ac) we will need to generate +5.0V, +10.0V, -10.0V, approximately +100V, approximately +200V, +2KV to +4KV, and 6.3Vrms. The total power draw for all of these supplies must be ≤4.5 watts from the battery in order to operate the monitor from a 12.0 volt, 1.5 amp-hour nickel-cadmium battery for the specified four hours. The least expensive, power efficient approach to this problem is to design one multiple output switching regulator to provide all of these voltages. Since the total power drain is low, the magnetics for this approach will be small and therefore not a problem.

Typically, in a multiple output supply, only one output voltage can be used to provide feedback. The supply with the tightest regulation and accuracy requirements (and preferably one of the highest power drains) is selected as the feedback voltage; the others are fairly tightly controlled by the effects of "core" regulation. One problem of this simple supply circuit is that all of the voltages except the feedback winding voltage can maintain only about 5% load regulation. By maintaining a fairly constant load and by designing circuits with good power supply rejection ratios, this limitation should not pose a serious problem.

The circuitry for this approach will consist of a pulse-width-modulated power supply regulator IC, external drive transistors in a push-pull configuration, one transformer with output windings to supply all of the required voltages, and rectification and filtering for all outputs. The efficiency of this approach should be between 80% and 90%.

Special considerations will be given to the high voltage supply. In order to supply 4KV, a large number of windings will be required on the transformer. This would result in high stray capacitance between adjacent wires, and increased inductance. In combination, this causes undesired resonances in the transformer. Another problem is that voltages of 4KV would be present on wires that typically have very thin insulation. This can cause voltage breakdown and subsequent component failure. This problem can be avoided by using expensive transformer manufacturing methods. However, both of these problems can be reduced by using a lower voltage winding and a high voltage multiplier.

Another potential problem with the high voltage supply is the mounting of high voltage components. One solution that will be considered is to encapsulate the transformer and all high voltage circuitry in a potted, possibly shielded assembly. This would improve performance in humid conditions, improve general reliability and increase the safety to the serviceman. In addition, it would move the high voltage circuitry away from sensitive low level circuits, and eliminate the mechanical restriction of mounting large components on circuit boards.

One other cost saving measure that will be considered is to drive the isolated front end power transformer directly from a winding of the main power transformer. This eliminates inefficiency, complexity, and the problems that can arise when power supplies operating at independent frequencies cause spurious beat frequencies that can interfere with low level signals or sensitive display components. The problem with this approach is that since the power frequency will be used for front end functions, it will have to be accurately controlled.

The battery charging time specification (14 hours) can be met by using a conventional trickle charging circuit which charges the battery at a constant low level current, regardless of battery condition. Faster charging times (5-7 hours) can be achieved by charging at higher currents for dead batteries and decreasing charging current as the battery charges. The cost for this circuitry is greater, and a slightly larger power transformer would be required. Unless otherwise directed by Corometrics, we suggest staying with the simpler trickle charge circuit.

3.37 Logic family

The majority of the logic functions of the 505/506 will be implemented with standard SSI and MSI logic. The functions of the monitor are specific enough so that no standard LSI logic IC's will meet the requirements of any large portion of the circuitry. The standard families of logic ICs are, in descending order of speed and power:

    ECL-Emitter Coupled Logic
    STTL-Schottky Transistor-Transistor logic
    TTL-Transistor-Transistor Logic
    LSTTL-Low-power Schottky Transistor Transistor logic
    CMOS-Complimentary Metal Oxide Semiconductor Logic

ECL and STTL use a lot of power and are faster that the
505/506 requirements. Some of the higher speed circuitry
may require the speed of TTL or LSTTL; since LSTTL uses
substantially less power than TTL, LSTTL will be used.
Most of the circuitry, however, does not require the speed
of LSTTL and can be implemented in CMOS. We will use CMOS
whenever possible since CMOS typically consumes one-thou-
sandth the power of LSTTL. (The monitor will require approx-
imately seventy-five SSI and MSI logic ICs. If LSTTL is
used with an average power dissipation of 30 mW per IC,
the total dissipation will be 2.25 watts, a considerable
part of the 4.5 watt power budget. If CMOS is used, with
an average power dissipation of 0.5 mW per IC, the total
dissipation will be 38 mW.)

3.38 Analog Circuitry

A large percentage of the 505/506 circuitry will be implemen-
ted with discrete analog circuitry consisting mostly of IC
operational amplifiers (op-amps) and voltage comparators.
The selection of op-amp or comparator for a particular cir-
cuit depend on factors such as accuracy and speed, but in
general, most circuitry will be implemented with low cost
op-amps and comparators with "standard" performance. Since
power dissipation must be minimized to attain the specified
battery life requirement, we will use low power programmable
op-amps instead of general purpose type (e.g 741) and low
power comparators. This will improve the power dissipation
of the 505/506 monitor by more than 0.75 watts. The addition-
al cost for using low power op-amps, such as the LM346, and
low power comparators, such as the LM339, will be about $5.00
in factory cost. Since this is a very reasonable power/cost
tradeoff, these parts will be used in the design of the
505/506. The LM339 comparator has been manufactured success-
fully for several years by many IC vendors and is a low cost,
general purpose, low power device. The LM346 was intro-
duced in 1978 by National Semiconductor as a programmable,
general purpose design and is currently sourced by at least
two other vendors. Where these general purpose components
provide inadequate performance, an appropriate part will
be selected, with low power as a prime consideration. We
expect this to be the case for less than 10% of the active
analog components.

4.0 Specifics of Design & Approaches

The specifications, goals, product guidelines, and product architecture have been established in the first three sections. The following sections define the design approach for each circuit. The design of each circuit will be discussed in terms of those product goals and specifications that are appropriate to it including functional characteristics, specifications, reliability, power, safety, size, cost, etc.

4.1 Front End Circuitry

The isolated front end circuit will be designed with particular attention to several important considerations: electrical performance specifications, appropriate patient safety standards, and defibrillator protection.

4.11 ECG

The ECG circuit consists of the following sections (depicted in figure 4.11A):

1) The patient cable
2) The input connector
3) Defibrillator protection circuitry
4) A dc amplifier with differential input, differential output, and common mode output.
5) A dc amplifier with differential inputs (which are the common mode output of the ECG preamp and floating ground), a high impedance to chassis ground output.
6) An analog multiplexer to time multiplex parameter voltages and output them to the isolation transformer.

These circuits comprise a two lead ECG circuit with high impedance from patient leads to chassis ground, and high common mode rejection ratio (CMRR). Normally, an isolated ECG circuit uses a third lead connected to the patient to eliminate common mode voltage. When monitoring neonates, however, it is desirable to use as few leads as possible. We will use an amplifier that controls the ECG preamp common mode voltage via a servo amplifier driving a high impedance to chassis ground, thus eliminating the third lead. The common mode signal is typically the 60Hz voltage induced on the patient due to his capacitance to hospital electrical wiring. This voltage, typically 20 volts to 40 volts, must be rejected by a ratio of 100,000:1 (100dB) to prevent 60Hz signals from interfering with the ECG signal.

Figure 4.11A Front End Block Diagram

POWER OSC.

DC POWER

MUX LOGIC

THERMISTORS

TEMP LINEARIZERS AND PREAMPS

T_1

T_2

DEFIB PROTECT

PRESS. TRANS.

PRESSURE DRIVE CHOPPER

FROM MUX LOGIC

PRESSURE PREAMP

$27M\Omega$

CHASSIS GROUND

SPARK GAP

GROUND DRIVE AMP.

ECG COMMON MODE

DEFIB. PROTECT

ECG AMP

LA

RA

ECG LEADS

RESP. CURRENT SOURCE

FROM MUX LOGIC

RESP AMP

RESP DEMOD

AUTO DC LEVEL

MUX

$-T_2$ $+$

$-T_1$ $+$

$-$ PRESS $+$

$-$ ECG $+$

$-$ RESP $+$

DEMUX

T_2

T_1

PRESS

ECG

RESP

CMRR on the order of 80dB is realizable using a differential amplifier with a gain of 10 (20dB) with a doubly balanced chopper and the isolation transformer to convert the differential signal on the isolated side to a single ended signal on the grounded side. This circuit has a strong advantage over the conventional differential input, single ended output amplifier, since its CMRR is not dependent upon amplifier characteristics or resistor matching. In fact, for low common mode voltage, with careful circuit and transformer design, the circuit could be made to provide the required 100dB of CMRR without additional circuitry. Unfortunately the differential input amplifiers and the choppers operate linearly only with input voltages within the range of their supply voltages. With common mode signals in the range of 20 volts to 40 volts, and amplifier supply voltages of only +5 volts to +10 volts, another approach must be used. The proposed solution is to drive the floating circuitry with a voltage such that the voltage difference between the patient and floating ground is minimized. This can be accomplished with an isolated amplifier whose output drives a high value resistor (>12 megaohms) to chassis ground.

The inputs to the amplifier are differential: one is the patient common mode signal, the other is isolated ground. This amplifier forces the isolated ground voltage to be near the patient voltage, allowing the ECG input stage to be within its linear operating range, and increases CMRR substantially. The ground drive amplifier output voltage will be in the range of the patient common mode voltage typically +40 volts. This is well within the capability of a discrete transistor amplifier. The high voltage power supplies for this amplifier must be generated by either voltage multipliers driven by the floating power transformer, or higher voltage windings on the transformer. The isolation between the floating circuitry and the chassis grounded circuitry can be maintained by a high impedance (typically several megaohms) from the high voltage amplifier output to the chassis ground.

Another problem of an ECG circuit is defibrillator protection. When a patient is defibrillated while connected to monitoring equipment, common mode and differential voltages on the order of 25KV can be expected. Without adequate protection the low noise, high impedance front end amplifier would be destroyed by this overload. The method of protection will consist of current limiting followed by voltage limiting, with excess energy shunted to chassis ground by a gas discharge device. Current limiting for ECG will be accomplished

by power resistors followed by voltage limiting via neon lamps. The resistors can be incorporated in the ECG lead set or on the preamp circuit board. The advantage of using resistors in the lead set is that much of the high voltage from the defibrillator is prevented from entering the monitor. The disadvantage to putting resistors in the lead set is that respiration detection is made considerably more difficult because the variation in patient impedance is an even smaller percentage of the total patient/lead impedance as seen by the monitor. In the 505/506, we will avoid incorporating resistors in the lead set unless the defibrillation protection proves to be a problem.

The neon lamps will limit the voltage seen by the ECG preamp to 70 volts; further protection will be required to avoid input failure. This will be accomplished by additional current limiting resistors and diode clamps to the power supply rails. The ground of the floating circuitry will be coupled to the chassis via a very low impedance spark gap during the defibrillation overload input. The spark gap acts as an open circuit until the voltage across it reaches 800 volts, at which time it acts as a very low impedance to chassis ground. This prevents the isolated ground form ever exceeding 800 volts with respect to the chassis ground allowing the isolation barrier, isolation transformers, etc. to be designed to withstand only 1KV instead of the full 25KV defibrillator potential.

The specifications call for the ECG input to operate with a dc offset of up to ± 300mV. Therefore the input differential amplifier gain will be limited to a factor of 10 to 20 to maintain an output within the constraints of the power supply voltages. The specified input noise, input impedance, frequency response, and CMRR are all attainable with off-the-shelf op-amps such as the LM308 precision low noise op-amp. This device operates at low power, and is fairly low in cost. An op-amp is preferred over a discrete transistor design because of its simplicity and the need for low output impedance to drive the transformer and chopper switch.

4.12 Respiration

The respiration front end circuit acts as a four wire impedance measurement instrument operating at a high frequency through the ECG leads. The first part of the circuit is a differential output, high frequency (20KHz) current source. The second part is a differential high frequency amplifier to measure the voltage induced across

the patient. The third section is a synchronous demodulator to provide a low frequency waveform proportional to chest cavity impedance. The low current, and therefore low induced voltage, presents special problems in attaining an adequate signal-to-noise ratio.

A current of 10μA will induce a voltage of 20mV across a typical patient impedance of 2000 ohms. A breath typically changes this impedance by only 1 ohm, resulting in a 10μV change in the 20mV input signal, or one part in 2000. For reliable signal detection, the noise level should be about 100 times lower, (~100nV) at the respiration carrier frequency.

Some of the factors that must be taken into account to attain an acceptable signal-to-noise ratio are the following:

1) Carrier frequency stability
2) Carrier current stability
3) Total ECG lead capacitance
4) Total patient circuit impedance
5) Preamplifier noise
6) Preamplifier gain stability
7) Demodulation errors
8) Effects of defibrillator protection circuitry

A slight change in the carrier frequency can cause an amplitude variation because the impedance of the ECG leads is capacitive. Deriving the respiration carrier frequency from a power supply oscillator (whose frequency is dependent upon temperature and load) is not good practice. It can be derived from the power supply, however, as long as the power supply is driven from a stable frequency source. This is the approach that we will take. The current amplitude must be stable to better than 0.005% over a short term. A precision clamping circuit will provide this stability.

The preamplifier gain and noise are the most difficult areas. To maintain a stable gain, a feedback amplifier will be used with differential input and output. The differential output driving a transformer through analog switches will maintain good CMRR and power supply rejection. Low noise transistors will be used for the preamp input stage. The defibrillator protection will be provided by series resistors and diode clamps to the power supply voltages. The respiration signal will be demodulated and conditioned (dc restored and amplified) on the isolated side and then multiplexed across the isolation barrier.

To give an indication of the sensitivity of the respiration circuit, consider a 1.0pF change in the lead capacitance due to a motion of the leads, etc. With a 20KHz carrier frequency, the capacitive reactance of 1pF is 80MΩ. This additional impedance across the normal 2000Ω patient impedance represents an error of 0.0025% - half of the error budget.

4.13 Pressure

The pressure front end circuit is defined by the parameters of the pressure transducer; the transducer will determine the gain, offset adjustment, low level performance, and the band width requirements of the circuitry associated with it. However, transducer excitation voltage requires some discussion. The transducer is a resistive strain gauge in a resistive bridge configuration. Its output signal level is 5uV/mmHg at 1.0V excitation level. The transducer excitation voltage can be dc or any waveshape, at any voltage level up to the level at which it begins to generate excessive heat. Typically a pressure transducer can use up an appreciable amount of power (at 5.0Vdc, a 300Ω transducer uses 83mW). Since that power is conditioned by both switching power supplies and inefficient linear amplification, the actual battery drain is about twice the transducer power. It is therefore desirable to apply the smallest possible signal to excite the transducer.

The lower the signal, however, the higher the required amplifier performance. This is important since at 5.0V excitation the transducer provides only 25mV per 1mmHg output. One method to reduce power and reduce amplifier cost as well is to drive the transducer from a square wave, or pulse waveform. This way, the amplifier can be a low cost ac coupled amplifier instead of an expensive, precise dc coupled amplifier. The multiplexing logic can provide the excitation timing and the multiplexing switching can provide the chopper demodulation. A precision reference amplifier is required for the transducer, and this amplifier can be easily pulsed by the multiplexing logic. The amplifier configuration will be differential input and output, implemented with op-amps. The low output impedance of the op-amps will drive the choppers of the demultiplexing circuit directly.

4.14 Temperature (Front End)

The temperature front end consists of a voltage reference, wheatstone bridge and amplifier. A YSI 44033 thermistor will be used. The thermistor will be linearized with a series resistor, producing a maximum error due to linearization of .02°C between 30° and 45°C. To minimize the effect of errors in the voltage reference or gain of the amplifier circuit, the other half of the wheatstone bridge is selected to produce 0V output for 37°C input.

There will be two separate temperature amplifiers and bridges, but they will share the same voltage reference. Multiplexing the low level thermistor signals to allow the use of a single precision op-amp will not be cost effective. The bridge voltage will be 0.5V keeping the self heating as low as possible while maximizing the voltage change per degree centigrade. This will minimize the error due to amplifier input offset.

The inputs to the temperature amplifiers will be protected from static sparks and filtered to eliminate noise.

4.15 Isolation Circuitry

There are five signals that have to be passed across the isolation barrier:

> ECG
> Respiration
> Blood pressure
> Temperature 1
> Temperature 2

The dynamic range requirements are somewhat different for each signal: the ECG requires about 54dB, and is not dc coupled; blood pressure has similar dynamic range, but this signal must be dc coupled; the temperature signals have a slightly smaller dynamic range, and are also dc coupled.

The isolation barrier requirements for respiration depend on whether the signal is de-modulated and ac coupled before or after the barrier. The 'raw' respiration signal has a dynamic range requirement of at least 80dB. The respiration envelope, after its dc component has been removed, has a dynamic range similar to the ECG.

The most important choice in the design of the isolation circuitry is whether to use a separate isolation device for each signal, or to multiplex all signals over one device. The relatively high cost of both opto-isolators and transformers makes the multiplexed approach very attractive. A straightforward time-multiplexing arangement will not be a problem except for the undemodulated respiration carrier. This signal has higher frequency components and its dynamic range is significantly greater than the rest. Since a multiplexed isolation scheme will have to be designed for the worst case signal, it is probably not economical to transmit the raw respiration carrier in this way. Therefore, we expect to demodulate and remove the dc component of the respiration signal in the isolated section. The one disadvantage of this approach is that the leads off condition will have to be detected in the isolated section and transmitted across the barrier explicitly, because this information is removed from the respiration signal during demodulation.

Crosstalk between analog channels is a potential problem with time division multiplexing. Experiments done by Corometrics have demonstrated that crosstalk can best be eliminated by allowing a "dead time" between demultiplexing states to allow for analog switching time.

We have considered both transformer and optical isolation devices. In either case, time multiplexing could be used. A simple digital CMOS circuit can be used to control the multiplex sequencing. A synchronization signal will be transmitted from the isolated section in order to synchronize the demultiplexer. The synchronization can be transmitted along with the other signals, using the same isolation device.

The opto-isolator scheme would use pulse-width modulation to encode the analog signals in a form the opto-isolator can handle without distortion. This will require a high-speed opto-isolator to give the required pulse-width resolution. Also, a high speed, low offset comparator would be required for the encoder. Pulse-width decoding would be accomplished using low-pass filters.

The transformer approach has some advantages, because it requires no precision or high speed analog components. Also, the transformer can accept differential-mode analog signals directly, without the need for an op-amp differential to single-ended conversion. This simplification would apply to the ECG amplifier, and possibly also to the pressure circuit. For these reasons, the transformer method is preferred, and is our recommended approach.

4.16 Power Circuitry

The floating power supply circuitry consists of two sections: grounded and isolated. The grounded circuitry will derive its power from the power supplies of the monitor, and drives the primary of an isolation transformer. The secondaries of the isolation transformer will be rectified and filtered to provide the necessary supply voltages of the floating circuits. A secondary function of the transformer is to provide the clocking signal for any multiplexing logic of the isolated circuitry. Since the isolated circuits will contain linear amplifiers, CMOS logic, pressure transducer drive circuitry, analog switches, and the high voltage amplifier for the two lead ECG circuit, it will have to supply several different voltages, each with different regulation and noise requirements.

The ECG preamp, pressure preamp and temperature preamp will all be implemented with monolithic op-amps. These amplifiers have good power supply rejection at low frequencies: it may be possible to operate them from unregulated ($\pm$10%), but well filtered symmetrical supplies. The CMOS logic and analog switches will be operated from the same supplies to simplify interfacing. These power supplies will probably be in the $\pm$7.0 volt to $\pm$10.0 volt range. The high voltage amplifier will require $\pm$60.0 volt supplies at very low currents (10-50μA). The alternative methods to generate these voltages are high voltage multipliers or higher transformer turns ratios. The least expensive approach will be selected during phase II.

The two remaining circuits require special attention. The respiration preamplifier will be implemented with discrete analog circuitry, and because of other design constraints may not have the same supply rejection as op-amps. The low level, high frequency nature of this circuit will probably require excellent power supply regulation, in which case the op-amp supply voltage will be fed into a linear regulator to provide the required regulated voltages.

The pressure transducer supply is also critical. To save
power and reduce the pressure amplifier cost, the transducer
will be operated from a very accurate pulsed source. The
problem is that current pulses on the order of 20mA at a
frequency of between 10KHz and 40KHz will be drawn from the
unregulated supply. These current pulses will have to be
adequately filtered to prevent noise from cross-coupling into
the other circuits. An L-C filter should provide the required
filtering.

4.2   Physical Processing Circuitry

4.21   ECG

The ECG processing circuit provides processed waveforms to the display and rear panel connectors. The parameters that are derived from the ECG signal are: averaged cardiotach, beat-to-beat cardiotach, QRS beep, high and low heart rate alarms, and a QRS LED.

The first function of the processing circuitry is to eliminate the dc level from the ECG signal. This is followed by a manual gain control to insure adequate gain for both display and subsequent processing functions. The waveform information is low pass filtered with cutoff frequencies of 40Hz and 100Hz for the display and rear panel connectors, respectively. The unfiltered waveform is applied to a slew rate limiter, which eliminates pace pulses, a matched (bandpass) filter designed to pass the frequency components of the QRS wave, and a trigger circuit which detects the QRS wave and generates a coincident QRS flash. This QRS flash signal is used to drive the QRS LED and the QRS beep. It also is used as the input signal to the beat-to-beat and averaging cardiotachs. The averaging cardiotach signal is applied to the alarm circuits and the digital parameter display circuitry for subsequent display of heart-rate on the CRT.

4.211   DC Level and Manual Gain Control

There are two approaches to the dc level control circuit. Both approaches are basically ac coupled amplifiers with provisions to increase the frequency of the high pass zero when excessive dc voltage exists. In addition, both circuits will be designed in conjunction with the high gain amplifier that boosts the ECG low level grounded signal to the high voltage level required for the ECG processing circuits.

The first type of circuit consists of an integrator in the feedback loop of an op-amp. This integrator maintains a constant output voltage dc level of zero volts. A comparator detects when the output of this circuit exceeds the dc limit voltages, and causes the integrator to charge more quickly by changing its time constant. This type of circuit is used in the 503/504. The disadvantage of this circuit is that a monostable between the comparator output and the integrator speed up is required to maintain stability.

The second approach consists of an inverting amplifier with a gain of several hundred and an ac coupled input. DC level restoring of the output is provided by zener diodes from the output to the input after the coupling capacitor. When the output exceeds the zener diode voltages, the diodes conduct, causing the coupling capacitor to charge quickly. This circuit is used by Hewlett Packard on the 78341/42 monitors. Because of its simplicity, relative to the 503/504 circuit, this circuit will be used as the fallback circuit for the 505/506.

The ECG gain to the display will be controlled by a front panel potentiometer. A resistor in the CCW leg of the pot will limit the minimum gain of the pot.

4.212 Filtering

Prior to digitization and further processing, the ECG signal must be band limited. The auto dc level circuit will provide a high pass filter with a zero at 0.05Hz. The display circuitry requires a low pass filter with a cutoff frequency of 50Hz, and the rear panel connector requires a cutoff frequency of 100Hz. The 100Hz filter will be provided by a two pole active filter, the 50Hz filter with a three pole active filter.

4.213 QRS Complex Filter

To calculate the heart rate, it is necessary to have a signal that occurs only once each beat. If peak detection of the unfiltered ECG signal were used, it would be difficult to prevent multiple triggering on different parts of the waveform, such as the T wave. A QRS matched filter having a frequency response which roughly matches the spectrum of a typical QRS complex, must be used to suppress the other components of the signal.

Corometrics has determined that good results can be obtained using a single stage active bandpass filter centered at 30Hz, with Q=1. This QRS filter is readily implemented using operational amplifier circuitry. We plan on incorporating the Corometrics design in the 505/506.

4.214 QRS Threshold Detect

This circuit must generate one digital pulse of fixed width for each QRS complex. The threshold must automatically adjust as the amplitude of the QRS changes. This threshold will be generated using a fast attack slow decay peak detector. The QRS is then detected by comparing the filtered ECG signal against a fixed fraction of the threshold. The final QRS pulse is then generated by firing a non-retriggerable monostable multivibrator from the comparator output. This yields a fixed pulse width, standard level QRS detect pulse.

4.215 Beat-to-Beat Measurement

The instantaneous, or beat-to-beat heart rate must be updated on every occurence of the QRS detect pulse. This circuit will calculate the inverse of the time between each pair of QRS pulses. Corometrics has suggested an instantaneous heart rate circuit, using precision resistors and capacitors to generate a time waveform that decays from a preset value approximately as 1/t. This circuit will be satisfactory for use in the 505/506, although we would not use the LF398 sample and hold because of its high power consumption.

Another approach to the beat-to-beat measurement operates by generating a high frequency pulse train with a frequency inversely proportional to the period between QRS pulses. The instantaneous heart rate is then generated by low pass filtering the high frequency signal. This circuit approach uses fewer precision components and analog switches than the 1/t capacitance decay circuit, and it does not require a precision

voltage reference. The accuracy of this 'rate multiplier' approach depends mainly on the ratio of two R-C time consultants; it may be possible to eliminate all adjustments. We are currently leaning toward this approach.

4.216 Averaging Cardiotach

The averaging cardiotach operates by low pass filtering the output of the beat-to-beat cardiotach. The low-pass filter must have a cutoff above the minimum heart frequency of 30 beats per minute (BPM) or .5Hz. An active filter with two poles will be required to achieve the specified settling time of less than 5 seconds and the required ripple rejection.

4.217 Alarms

The low and high heart rate alarms are generated by comparing the user selected limits against the output of the averaging cardiotach. A time delay will be applied after the comparators before triggering the alarm, so that if the heart rate goes beyond the limits for only an instant and then recovers, the alarm will not go off.

4.22 Respiration

The respiration parameter will be monitored using standard impedance pneumography techniques. An isolated ac current of 200uA peak-to-peak operating at a carrier frequency of approximately 20KHz will be used to sense changes in the thoracic impedance. The oscillator design will insure that changes in power supply voltage do not induce a false respiration artifact.

The carrier frequency voltage developed across the chest electrodes will be amplified and passed through a synchronous demodulator. It is felt that the increased complexity of this technique versus a more simple rectifying demodulator is warranted due to the improved immunity to spurious signals.

4.221 "Leads Off" Detect

The output of the demodulator is a signal whose dc level is proportional to the average value of the thoracic impedance. This level will be monitored with an analog comparator to ensure that measured impedance is below a limiting value of 4K ohms. This figure represents the total of patient impedance,

electrode connection, and protection resistors within the
cable itself. If the measured impedance rises above the
4K limit, it is assumed that the electrodes are making poor
contact. In this event, a "leads off" alarm will be gener-
ated irrespective of the condition of the ECG circuitry.

4.222 Filtering

Besides "leads off", the demodulated impedance signal is
used for two different functions. Firstly, the impedance
variations can be displayed on the CRT of the monitor as a
raw waveform. Because the variation of impedance is so
slight ($\approx 1\Omega$) compared to its base level ($\approx 2K\Omega$), an ac
coupled high gain stage is required to extract the useful
signal. This circuit will also include a bandpass filter
with a high frequency limit of 4Hz to help reduce noise
(There being no pertinent information at frequencies above
this value) and a low frequency corner of 0.1Hz. This latter
figure is a compromise between allowing for rapid baseline
recovery without disregarding pertinent respiration infor-
mation.

4.223 Auto DC Level

With a low frequency cutoff point of 0.1Hz, moderate shifts
in baseline impedance due to electrode motion or body move-
ment could take several seconds to settle through the ac
coupled gain stage. Therefore an automatic dc level res-
toration circuit will be used. The function of this will
be the rapid restoration of baseline voltage in the event
of overscale changes in impedance. This circuit will operate
automatically without the need for operator intervention.

The respiration waveform will be displayed on the CRT with
a gain which may be adjusted through a control on the front
panel. This control effects only the display size and does
not affect the threshold level of the breath detection
circuitry.

4.224 Breath Detection

The second function of the respiration circuit is to extract
breath events from the waveform. This information is used to
determine the respiration rate and to sound an alarm if apnea
is suspected. The breath detection circuitry examines whether
the respiration signal has traversed a certain span of imped-
ance change. This action is then interpreted as a breath
event and the information is passed on to the rate counting
and apnea circuits. The key to proper operation of the breath

detection circuit is the choice of a suitable threshold level. There will be two modes of operation for this circuit. The first is a manual mode in which, the breath threshold level is fixed at 0.6cm on the display. The second mode of operation is to dynamically adjust the threshold level based on the respiration signal excursions, the present threshold level, and present information from the cardiac artifact detection circuitry. If the threshold is set too high, real breathing will be ignored and false apnea alarms will result. On the other hand, if the threshold level is set too low, false triggering may cause episodes of apnea to be missed, especially if the cardiac artifact detection circuitry does not adequately reject cardiac signals. The threshold level will operate on a breath-by-breath basis. As each breath is observed, its size will be examined to determine whether to raise or lower the threshold level. However, the percentage change in threshold level will be limited on a per breath basis. In other words, a single large excursion will not be able to increase the threshold level by a large factor (2, 3 or more as in Hewlett Packard and other monitors). With a per breath increase limited to a factor of, say 25%, it would take 4 large excursions to roughly double the threshold size (The actual value of increase will be determined empirically). This action should decrease the incidence of false apneas due to a single large excursion forcing the threshold value to an incorrectly high level.

If the signal does not cross the present threshold level, the level will be permitted to decline. However, the rate of decline will be slower than that of competitive monitors. (For example, the Hewlett Packard 78342 neonatal monitor allows its respiration threshold to decline with an RC time constant of 7.8 seconds. This means that during a 15 second episode of apnea, the threshold will decline to about 1/7 of its original value. This rapid change in level is undesirable and leads to false triggering problems). It is felt that the above described method of limiting rapid increase in threshold level will result in a more representative or "correct" level; it will therefore be possible to allow the level to decay more slowly. Also, it may be desirable to control the rate of threshold decline in tandem with the setting of the apnea duration alarm. The objective of this would be to allow a rate of decline in respiration threshold which would be a function of the apnea alarm setting rather than absolute time.

The auto-threshold level will be allowed to vary over a range of 0.2Ω to 3.0Ω, a factor of 15:1.

4.225 Respiration Rate

As each breath event is detected, it will trigger a rate-meter circuit which will maintain a running average of the respiration rate. This rate will be displayed on the CRT face. In the event of an apnea alarm, the averaging filter will be reset forcing the ratemeter to zero.

4.226 Respiration High Limit Alarm

There will be a user-setable alarm for high respiration rate. This control will be a slide pot and have a range of 10 to 100 breaths per minute.

4.227 Improved Apnea Alarm

There will be no low limit alarm per se on respiration rate. This function will be taken care of by the apnea alarm, which will function as a timeout device. The apnea period can be set by a user control in the range of 10 to 20 seconds. If there have been no respiration events for the indicated period, the alarm will sound. However, the actual operation is a bit more complicated than this would indicate. Rather than completely resetting the timeout mechanism with each breath event, the equivalent of 4 seconds are subtracted from the timer. Thus with the apnea alarm period set to 20 seconds, an alarm would sound after a 16 second apnea, a single breath event, and an additional 10 seconds of apnea.

4.228 Cardiac Artifact Rejection

A common problem in impedance pneumography is the fact that cardiac activity creates an impedance variation which can be misinterpreted as rapid, shallow breathing. A foolproof, accurate, automatic determination of whether an impedance waveform represents respiration or cardiac artifact has not been accomplished to date. Improved operation in this regard will be a primary focus of the respiration development effort. There are two general approaches to reduce this problem.

The first is to estimate the size of the cardiac signal and make certain that the respiration threshold level is at least several times larger than the perceived artifact. This prevents false triggering, but lowers the circuit sensitivity.

The second method involves no modification to the threshold level, but rather looks for coincident timing between ECG and respiration flashes. If such is found, the apnea alarm is then sounded.

Experimental investigation along the lines of these techniques should yield an algorithm with improved performance over current competitive designs. Also, the improvements made in automatic setting of the threshold level should hopefully decrease reliance on flawless cardiac artifact rejection action.

4.23 Blood Pressure

The blood pressure signal is a dc voltage and must be dc coupled through all circuits. Processing for this signal consists of accurately zeroing the transducer and amplifier output signal, filtering the signal to remove any high frequency noise, and accurately controlling the waveform gain to the CRT circuitry. There are four parameters that will be derived from the pressure waveform. Three of these parameters, Systolic, Diastolic, and Mean, are in the form of analog voltages. The fourth parameter, Excess Pressure alarm, is a digital signal indicating that an operator is using the pressure transducer incorrectly. The digital signal activates the audio alarm.

4.231 Pressure Filtering

A low pass filter stage will preceed all other pressure processing. This filter will eliminate any multiplexing spikes or other high frequency noise present on the pressure signal. Since the signal is peak detected to determine Systolic and Diastolic pressures, any noise spikes present would affect these readings. The pressure filter will be a two pole low-pass butterworth filter with a cut-off frequency of 40Hz. The output of this filter will be a normalized amplitude pressure waveform.

The stage following this filter will be the auto-zero circuit, which will compensate for offset errors generated by the transducer and any preceding circuitry. The auto-zeroed signal is sent to the parameter circuits, for processing the variable gain stage, for display and output gain and to the rear panel.

4.232 Pressure Auto-Zero Circuit

The auto-zero circuit eliminates the offset errors of the pressure transducer, preamplifier and filtering circuits, providing a zero pressure indication for zero input pressure. A digital counter and a D/A converter is sufficient for this function. The operator will open the pressure transducer to atmospheric pressure and press the auto-zero button. This will reset the counter to zero, and start up-counting. The counter output is fed to the D/A input, which generates a voltage proportional to the count. An offset voltage is added to the D/A output so that zero count will correspond to -100mmHg, and the full scale count will correspond to +100mmHg. The D/A output will be algebraically added to the pressure signal, and a comparator will detect when this sum exceeds zero. At this point, the counter will be stopped and the current count maintained until the process is repeated. The counter will be a CMOS ripple counter, operating from a submultiple of the main system clock. Assuming a 25KHz rate, a count of 256 will require 10ms to zero. The D/A converter will be an inexpensive (+0.5LSB) 8-bit CMOS DAC such as the Analog Devices AD7523JN. This will provide a zeroing error of +0.8 mmHg worst case. The reference for this DAC will be provided from a system master reference. CMOS logic will control the resetting of the counter and the counting. The 25KHz rate should be slow enough such that the amplifiers and comparators will settle between counts; if not a slower rate will be used.

4.233 Pressure-Gain Control

The gain control circuit increases the gain of the pressure channel in two discrete increments to allow a user to increase the display size when the pressure transducer is used to measure venous or other low amplitude physiological pressures. The gain stage will consist of an amplifier with switch selectable gains of X1.0 and X2.0 to provide full scale pressures of 150mmHg and 75mmHg, respectively. The output of this amplifier will go to both the desplay circuitry and the output connector.

Assuming a pressure transducer sensitivity of 5 V/V/mmHg, 5V excitation and a maximum output of 3.0V at 150mmHg, the gain and signal level distribution will be as follows (X1 gain setting):

Stage	Signal Input Level	Gain	Output
Transducer @ 150mmHg	5.0V	5V/V/mmHg	3.75mV
Isolated Preamp and Multiplexor	3.75mV	400	1.50V
Filter & auto-zero	1.50V	2.0	3.0V

The signal will be present for all internal processing at
this level (3.0V=150mmHg). This will allow the high pres-
sure alarm of 300mmHg to operate at a threshold of +6.00V,
well within the operating range of a comparator with +10.0V
supplies. At this signal level, subsequent op-amp offset
voltages will not contribute significant errors. The pres-
sure waveform at the output connector has an accuracy speci-
fication of $\pm$3%. Although most of the gain stages can
maintain a $\pm$0.2% accuracy with 0.1% resistors, the isolation
barrier loss and accumulated stage gains may exceed the 2%
limit, necessitating a gain porentiometer.

4.234 Pressure - Mean Filter

The mean pressure value can be extracted from the pressure
signal with a low pass averaging filter which adequately
attenuates the heartrate frequency. Assuming a full range
pressure waveform of 100mmHg and a desired ripple of 1mmHg
at a heartrate of 40BPM, 40dB attenuation is required at
0.66Hz. To achieve this attenuation requires a two pole
low pass filter at 0.10Hz, a three pole filter at 0.20Hz,
or a four pole filter at 0.40Hz. The response times for
these filters are 12 seconds, 6 seconds, and 3 seconds,
respectively. Because this parameter is not an extremely
important one, a response time of 12 seconds would probably
be adequate (suggesting the use of the least expensive, 2
pole filter). However, since the other pressure parameters
update every two seconds, the mean pressure reading should
follow these readings reasonably well. Although still a
compromise, the three pole filter will be used, since it
can be implemented with one op-amp while the four pole
circuit requires two. In addition to a cost and board
area penalty, two op-amps introduce twice the offset error
of one op-amp.

4.235 Pressure – Systolic and Diastolic Peak Detectors

The systolic and diastolic peak detectors provide the maximum and minimum values of the pressure waveform. The peaks of these waveforms can be detected using conventional active peak detector circuitry. There are several possible methods of resetting these detectors, including:

1) Reset systolic on diastolic peak and vice versa. The signals must be sampled and held between resets.

2) Reset on a display update signal.

3) Use two peak detectors, each one reset on every other peak. The output is the analog maximum of both detectors.

Method 1 is used by Tektronix in the 413A. Timing signals corresponding to systolic and diastolic peaks are detected and used to control serial sample and hold circuits (S/H) such that the systolic peak is held when the systolic peak is detected. When the diastolic peak is detected, the held systolic peak is sampled and held again. The output of this second S/H is the systolic value. The reason for the second S/H is that during the sampling period of the first S/H, the value changes substantially. An equivalent but reverse polarity circuit derives diastolic pressure. The sampled and held output must then be filtered to eliminate glitches between samples. This method requires 12 op-amps and 4 switches for implementation.

Method 2, used in the 503/504, requires a signal from the numeric display circuitry to reset the peak detectors after the values have been digitized. This assumes that at least one pressure pulse comes between each display sample interval, and that continous "systolic" and "diastolic" signals are not required for any other reason. This method performs well, and is low in cost.

Method 3 consists of two peak detectors each for systolic and diastolic measurement. A logic signal is derived from the heart rate divided by two to control the resetting of the peak detectors. Each of the two peak detect circuits is reset on alternate QRS complexes, so that one always has the previous peak value stored in it. An analog maximum circuit then selects the maximum value of the diastolic or systolic pressure. This technique depends upon an external logic signal corresponding to a fixed point in the cardiac cycle. Monostables and flip flops insure that the systolic

and diastolic peak detectors are reset at the appropriate times. This circuit is used by Hewlett Packard in the 78340 series monitors. It is fairly expensive, requiring 8 op-amps, 4 switches, and several CMOS IC's.

The approach we recommend for the 505/506 monitors is method #2 since it is the simplest, least costly and performs adequately. However, it requires a suitable signal from the display circuitry. The complexity of generating that signal will be compared with the added complexity of methods 1 and 3 before a final decision is made.

4.236 Excess Pressure Alarm

A fixed level comparator will detect when the normalized pressure waveform exceeds approximately 300mmHg. This will Trigger an alarm for the duration of the time that the pressure exceeds 300mmHg. This alarm's volume will not be affected by the "alarm volume" control.

4.24 Temperature Processing

The temperature signals, after being recovered from the isolation section, are dc signals linearly proportional to temperature. Before being applied to the numeric A/D converter, a dc offset and scale factor must be applied, since the temperature front end operates with it's output range centered around zero volts. The offset will be applied with analog circuitry, rather than digitally, since it is the least expensive. The temperature signals will also be low pass filtered by this stage.

4.25 Other Physiological Processing Circuitry

4.251 Alarm Logic

The conditions that can cause an audio alarm are the following:

    High heart rate
    Low heart rate
    High respiration rate
    Apnea (loss of respiration)
    High pressure

When any of these conditions exist, an audio alarm tone is generated. The minimum time for an alarm tone will be two seconds to allow very short alarm conditions to be heard for a detectable period of time. When a function causes an alarm, the digital display corresponding to that parameter flashes on the CRT. The alarm can be temporarily disabled by pressing the momentary "Alarm Off" button. This causes the alarm tone

to be disabled for two minutes; a light adjacent to the
switch flashes at a 1Hz rate while the alarm is disabled.
The alarm is re-enabled either manually by the operator
pressing the "Alarm Off" button again or automatically
upon termination of the two minute interval. The alarm
volume can be adjusted by a rear panel control. This
control has an OFF switch in the fully CCW position. In
this position, the alarm sound is completely eliminated,
and the front panel ALARM OFF light flashes. The alarm
has a minimum sound level when the control is not in the
fully CCW position.

The circuitry to implement these functions will be mostly
CMOS logic. A J-K flip flop will provide the alternate action
of the alarm off button. A two minute digital monostable
will be triggered when the alarm is turned off, and the
falling edge of the monostable's two minute pulse will reset
the flip flop to the alarm-on state. When either the alarm
flip flop is in the off state or the rear panel alarm po-
tentometer is in the off position, the alarm off light flashes.
The flashing of all lights and displays will be at approximately
1Hz and derived from the display timing logic.

The circuitry to flash the CRT numerics associated with an
alarm will inject the 1Hz flash signal into the intensity
blanking circuit during the display of the appropriate digits.
Since the digit display circuitry simply reads out the digit
RAM, logic will be required to decode the digits for heart
rate, respiration rate, and systolic pressure, to flash the
appropriate digits. One decoder IC will provide this function.

4.252 Audio and Light Circuits

Two audible indicators and several LEDs will be provided in
the 505/506. The audible indicators are the alarm sound,
and the QRS beep. Hewlett Packard has spent a significant
amount of time and effort in attempting to provide as much
information as possible through the QRS beep. For example
the 78312 provides a change in beep pitch as a function of
heart rate. This seems like a good idea, but in a hospital
situation where there are many monitors in the same room
(such as a neonatal ICU) this can cause incredible confusion.
In addition, when a patient has a rapidly varying heart rate,
the beeper sounds like a random tone generator, providing no
useful information. Nurses reactions to this beeper are unan-
imously negative.

The technique that will be used in the 505/506 will be to provide a high frequency QRS beep and lower frequency alarm sound. The QRS beep is generally listened to on mostly a subconscious level, and is rarely used at full volume. Since this tone is on continuously, and is not intended as an attention signal, a sine wave will be used, resulting in a pleasing sound.

The frequency of the QRS beep will be about 1KHz. The alarm sound will be generated separately, at about 500Hz, which is close to the ear's peak sensitivity. The waveform that will be used will be either a square wave or a triangle wave. Both of these waveshapes contain audible harmonics; the square wave containing the most, the triangle wave being more pleasing. The harmonics will make the alarm more of an attention getting sound. Both waveforms will be generated separately and will drive the speaker simultaneously, allowing an operator to hear QRS beeps during an alarm. The penalty of supplying separate wave shapes is that slightly more complex circuitry is required. The 1000Hz and 500 Hz tones will be harmonically related to provide a pleasing relationship between tones. The 1000Hz tone will be filtered in a two pole filter to convert it to a sine wave. The gating signal for the QRS beep (QRS flash) will have limited rise and fall times to reduce the click sound at the beginning and end of the tone. The audio amplifier for the speaker will be a class B output stage on the output of an op-amp to provide efficient operation and low quiecent current. The amplifier output stage will be run from the +5.0V supply and will provide a maximum power of 200mW into an 8Ω speaker.

LEDs are used to indicate several functions on the 505/506. They are:

    Alarm Off
    QRS Flash
    Respiration Flash
    Leads Off
    Line

The control signals for these indicators will be sent to the front panel PC board as CMOS logic levels. The LED driver circuit will be on the front panel PC board and will drive the LEDs from the +5.0V supply in order to use as little power as possible.

4.3   Display Control Circuitry

4.31   Waveform Display

The following discussion is based on the use of a 16K x 1 dynamic RAM chip for the storage of both analog traces. This approach is the most complicated in timing and support logic but yields the best power/cost/space/ and risk trade-off of of the possibilities presented in Section 3.34. The same basic scheme, with certain simplifications, could be used to support other memory devices.

Figure D-A shows a block diagram for the display memory and system timing section based on using a single 16K dynamic RAM. The power and chip count for this implementation are as follows:

Chip Count:

	Qty	Pins	Logic
	15	16	CMOS
	2	16	LSTTL
	1	16	RAM
	18		

Power Dissipation:

			(Intel 2118)	
RAM	-	90mW	-	250mW (4116 type)
LSTTL	-	50mW	-	50mW
CMOS	-	10mW	-	10mW
		150mW		310mW

For comparison, the statistics for the shift register (SR) approach are as follows:

Chip Count:

	Qty	Pins	Logic
	16	8	SR
	18	14,16,24	CMOS
	24		

Equivalent 16 pin count =

Power Dissipation:

SRs	-	480mW
CMOS	-	10mW
		490mW

The statistics for a 4816(2Kx8) dynamic RAM are as follows:

Chip Count:

	Qty	Pins	Logic
	1	24	4816
	17	16	CMOS
	20		

Equivalent 16 pin count =

Power Dissipation:

RAM	-	65mW
CMOS	-	10mW
		75mW

We will probably use the 4816 dynamic RAM since it simplifies system design and reduces power.

4.311 System Timing

The slowest repetitive event in the display control system
is the scanning of one complete screen, including both
numerics and waveforms. This will take exactly 1/60 second
This interval is divided into four equal phases: W1, W2, N1,
and N2. N1 and N2 are for the numeric display, which takes
1/120 second; W1 is for waveform #1 (ECG or trend) and W2 is
for waveform #2 (pressure or respiration).

During one screen refresh, eight new values must be entered
into the RAM memory (four for W1 and four for W2). Because
the A/D conversions must be periodic, and to avoid scratch-
pad memory, four of the memory writes will occur during N1
and N2. Memory refresh must be maintained during N1 and N2.
To save power, the memory can be in standby during N1 and
N2, except for the four writes and the refreshing.

The overall memory cycle is controlled by a counter (counter
'A') which counts 962 sample-times during each of the four
phases. This allows for 960 reads and two writes during each
phase, satisfying the requirements for W1 and W2. A second
counter, (counter 'B') generates the word address for the RAM.
By having counter B count modulo 960, the proper memory word address
one count during 'A's cycle, the proper memory word address
for both reading and writing is generated without the need
for multiplexing or parallel loading either counter. Figure
D-B shows how these two counters relate to the screen dis-
play.

4.312 Waveform Memory

Each word access to the memory requires 1/240 x 962 seconds
(approximately 4330ms). During this time, eight individual
memory operations, either read or write, must be performed.
This type of bit-serial operation lends itself to the use
of page mode of RAM cycle. Each of the bit accesses within
the page mode cycle are simpler to control and take less time
than complete RAS-CAS cycle.

In order to implement the control for the page-mode RAM
cycles, each word access will be split into ten states.
Figure D-C shows the simplified memory timing diagram. There
are eight states for the bit-accesses, one for generating RAS,
and one for resynchronizing the state of the A and B ripple

counters. The ten-state sequence also determines the time for loading the data serial-to-parallel and parallel-to-serial converters.

An important circuit issue concerns the 10-to-5 volt conversion. CMOS circuits, including the A and B counters, and the memory ten-state controller, must be at 10 volts to provide adequate speed. The RAM requires 5 volts.

The seven RAM address signals, to provide the separate row and column addresses, will come from a 2-to-1 multiplexer. If this is implemented with LS-TTL, then the level conversion and multiplexing can be done in one step. The other inputs and outputs (RAS, CAS, WRITE, DIN and COUT), must be level shifted separately.

In order to achieve mimimum power, most RAM cycles will be inhibited during phases N1 and N2. Only the first cycle on each new row address will be allowed to run (for refresh). Of course, the four memory writes during N1 and N2 can not be inhibited.

4.313 Freeze and Slow Speed Logic

The waveform freeze mode can be easily implemented by adding another 'stall' state to the B counter sequence (see Figure 4.31B). Also, the memory write signal must be disabled during the freeze. The slow-speed mode can be implemented as a series of 'freezes' followed by a one-cycle non-freeze. This must be controled by a modulo 50 counter since the ratio of normal to slow speed is 50-to-1.

4.314 CRT Sweep Control

The CRT sweep retrace will be controlled by the memory control system during phases W1 and W2. The retrace signal is derived from the A counter. Also, the Z-axis is blanked during the two memory write operations at the end of each line, during W1 and W2.

4.315 Waveform A/D Control

The waveform A/D 'Convert' signal is derived from the A counter and is synchronized to the proper state of the memory ten-state controller. This causes the data to be changed at the input serializer at the instant it is needed. A single-word FIFO (i.e. an eight-bit register) is needed to save the conversion result completed during the middle of

W1 or W1. Note that this FIFO function required a 4-word
scratch-pad RAM in the 503/504 shift register implementation.

4/316 Waveform A/D

The requirements for the Waveform A/D present no special pro-
blems. The A/D must digitize two different waveforms every
4ms, or 2ms per digitization. Front panel switches select
which two waveforms are digitized; the waveform display cir-
cuitry determines which of the two waveforms is to be digi-
tized in a given 2ms slot.

The A/D accuracy requirements are well defined: 8-bit CRT
resolution and linearity, with +2mmHg out of 300 mmHg zero
accuracy ($\pm0.67\%$). One of the least expensive methods to
implement this converter would be with a single slope con-
verter. A ramp and a counter are started simultaneously.
The ramp is compared to the input signal by a comparator,
and when the ramp exceeds the input, the count value is
equal to the digitized value. Since the digitization is syn-
chronous with the display logic, the display counters can be
used to provide the counting functions, and the comparator
output can be used with an eight bit latch to store the dig-
itized value. The waveform write logic then reads the latched
value, and the process is repeated for the next value.

Although this technique is similar to the one used in the
503/504, there are some inherent problems. First, the
accuracy depends on a precision ramp signal and therefore
a precision capacitor (better than 1% tolerance). A less
precise capacitor can be used in conjunction with an adjust-
ment, but this offsets the cost advantage of the circuit.
A better approach is to use a low cost eight bit CMOS D/A
converter instead of a ramp. The D/A can be driven directly
from the counter, and can derive its reference from a main
system reference. Another advantage of the D/A over the ramp
is that resetting the D/A is almost instantaneous, while
resetting the ramp requires a significant amount of time.
This simplifies the control logic and timing. The current
output of the D/A can be summed directly with the input vol-
tage using a resistor; the comparator can be connected be-
tween this sum and ground. This makes the comparator less
critical than if it is comparing two random voltages. The
speed requirement for this circuit is 256 levels in 2ms or
8ms per bit. This is well within the capabilities of CMOS
D/As and low speed, low power comparators. The control logic
will allow D/A and comparator settling time before latching
the count. This will prevent D/A glitches from causing
errors.

This approach is less expensive than a successive approximation A/D by virtue of the fact that a counter is much less expensive than a successive approximation register. It is eight times slower than a successive approximation A/D, but it is adequate for this application.

4.317 Waveform D/A

The waveform D/A accepts eight bit digital waveform data from the waveform memory and converts it to an analog voltage for the CRT vertical deflection amplifiers. The requirements of this circuit can be met at low cost with a CMOS D/A and a fairly high speed op-amp.

A reconstruction filter similar to the one used in the 503/504 will follow the D/A. This filter will be a "Paynter" type filter, consisting of a notch filter in series with a low pass filter.

4.318 Waveform Sweep

A linear ramp horizontal sweep voltage is required to display the contents of the waveform memory on the CRT. This ramp can be generated least expensively with an integrator and a reset switch. The integrator will consist of an inverting op-amp with a feedback capacitor and a constant current input. Control to start and reset the sweep will be through a CMOS switch. A logic signal generated by the waveform read timing will provide sweep control. The same control signal will blank the CRT beam during sweep reset.

4.319 CRT Control Switching

During 8ms of a 16 ms CRT cycle, the waveform circuitry has control of the CRT X, Y, and Z inputs; during the other 8ms, the parameter control circuitry has control. The CRT control switching circuitry switches control between the two sources at the appropriate time. A control signal is generated by the waveform logic to provide control, and the X and Y control voltages from the waveform and parameter circuits are multiplexed with CMOS switches. The Z-input is handled slightly differently. There are two components of the Z-signal. The analog intensity voltage for the waveforms is constant, and the analog voltage for the parameters is determined by a lookup table consisting of analog switches. This lookup can easily be disabled during waveform display and a constant

value used instead. This would provide the intensity vol-
tage switching function at minimun cost. The digital blank-
ing signals for the waveform and parameter displays will be
gated with digital circuitry.

4.32 Parameter Display

The implementation of the selected stroke character genera-
tion technique (Section 3.35) is detailed in the following
sections. Basically, the circuit will consist of an A/D con-
verter, logic to control the A/D and the writing of digital
data into memory, logic to read the dat out of memory at
the right point in the display cycle, and the hardware nec-
essary to convert the data to the X and Y voltages necessary
to form the characters on the CRT (see figure 4.32).

The display memory will be a 16 x 4 bit CMOS RAM with one
BCD digit each per fifteen displayed digits plus one spare.
Its address will be controlled by two sources: the CRT
display hardware and the A/D converter. During the 8ms period
when the numerics are being displayed, the display hardware
controls the reading of the RAM. During the 8ms period
when the numerics are not being displayed, the A/D can write
new val es into the RAM.

4.321 Parameter A/D

The parameters that will be digitized are the following:

1) Heartrate   30 to 240 BPM
2) Pressures   50 to 250 mmHg
3) Respiration rate   0 to 150 BPM
4) Temperature   30.0°C to 45.0°C

The display on the CRT will be organized as five sets of
three digits each. The sets of digits will have the follow-
ing formats:

PARAMETER	RANGE	DISPLAY
Heartrate	0 to 9	00 to 09
	10 to 99	10 to 99
	100 to 299	100 to 299
Respiration Rate	0 to 9	00 to 09
	10 to 99	10 to 99
	100 to 299	100 to 299
Pressures	-50 to -10	-50 to -10
	-9 to -1	-09 to -01
	0 to 299	Same as heartrate
Temperatures	30.0° to 45.0°	30.0 to 45.0

The rules for the display are therefore as follows:

1) Two digit values displayed in right most positions
2) Only hundreds column 0 is blanked
3) Negative displays are limited to two digits
4) Negative sign uses left most digit position
5) Right most digit is moved over slightly to accomodate decimal point for temperature display.

Because of the decimal digit organization of the display, BCD code is the best format for the digital numerics data. Therefore the A/D converter will generate a digital value consisting of three BCD digits. There are several methods of accomplishing the BCD A/D conversion. Because of the low conversion rate requirement (seven conversions in two seconds or 0.286 seconds per conversion) dual slope conversion will be used. The required resolution is one part in 500; a commercially available 3½ digit dual or quadslope converter will suffice. However, the cost for a commercial A/D is $10.00 and the parts cost for a discrete A/D is $5.00. If substantial board area can be saved, the commercial A/D will be used. The design is straight forward, except for handling negative input signals. Two solutions to this problem are:

1) Use an up/down counter that is initialized at a value of negative full scale. It counts down to Ø, then logic detects Ø and causes the counter to count back up to full scale. The sign is determined by whether Ø was reached or not. The accuracy of the Ø depends on the matching of two 0.1% resistors.

2) Use analog hardware to detect the sign of the input signal and to switch the reference or input polarity.

Considering the accuracy requirement, either of these approaches is feasible. The output of the A/D circuit will be three BCD digits and a sign bit. Discrete logic will force the MSB to be a blank code if the digit is a "0" or a minus sign code if the polarity is negative. Since the BCD code uses four bits (16 possible codes) and only ten discrete codes, two of the six unused codes will be used for the minus and blank codes.

The completion of a conversion will set a flag to indicate to the display buffer write logic that it may pickup the digitized value and store it into the RAM.

4.322 Character Memory Logic: Write

The character memory will be a 16 x 4 bit CMOS RAM. These
parts are readily available and inexpensive. The fifteen
displayed digits will be stored in the RAM as BCD digits
with minus and blank as two of the six unused BCD codes.
When the data available flag is set at the beginning of the
8ms. waveform display cycle, the RAM write logic initiates
a write cycle.

A write cycle performs two functions. First it places the
appropiate digits from the A/D into the appropriate addresses
in the RAM. Second, it initiates sending the output of the
BCD digits to the rear panel system connector. The fact
that the display memory uses only five parameters, and the
system connector needs all seven complicates the circuitry.
The easiest solution is to inhibit writing into the memory
when an undisplayed parameter is digitized. This can be done
by inhibiting the RAM write pulse and the RAM address in-
crement when the RAM addresses corresponding to the "Select"
digits on the CRT are addressed and the parameter digitized
is not the parameter selected.

The sequence of a write cycle is as follows:

1) At the beginning of waveform display (Non-character
   display) A/D done flag is checked. If set, a write
   cycle is initiated, and the RAM address MUX is set
   to write.

2) If parameter count =0, reset write counter
3) Set the digit mux to 0 (MSB)
4) Output to system connector; write digit to memory
   if write inhibit is 0
5) Increment write count if write inhibit is 0
6) Increment digit mux, check for 3
7) Repeat 4) - 6)
8) Initiate new conversion

The timing for the write logic will be provided by the wave-
form memory clocking signals. The time for an A/D conversion
will be less than 200ms. If the write cycle requires a max-
imum of two complete CRT scans (1/60 second each). The max-
imum conversion cycle time is 0.24 seconds, allowing 8 com-
plete conversion cycles in the two second display update time.

4.323 Character Memory Logic: Read

The reading of the character RAM is controlled by the same
timing signals as the waveform display circuitry. Eight
milliseconds is available for the character display. The
eight milliseconds used for character display are divided
between sixteen characters (one will not be visible). Since
each character requires one address of the 16 x 4 bit RAM,
a four bit counter will sequence through the memory at 0.5ms
per address, providing 0.5ms to display each character. The
signal which distinguishes between waveform and numerical
display cycles will be used to switch the RAM address from
the read address to the write address.

4.324 Character Generator

The character generator circuit takes a character code from
the parameter read logic and converts it to the X, Y, and Z
voltages required to write the character on the CRT. To gen-
erate stroke characters, a character set consisting of char-
acters formed by discrete line segments is designed. This
character set is digitized by hand, and the data that repre-
sents the segments for each character are stored in a ROM.
By organizing the data as sixteen possible characters of six-
teen arbitrary segments each, the data will fit in 256 words
of ROM. Each word is used to generate X, Y, and Z values
for the strokes of each character.

There are two basic methods of generating stroke characters;
constant time vectors and constant rate vectors. Constant
time vectors are drawn in the same time period, independent
of length. Constant rate vectors are drawn at a constant
speed across the CRT face. The problem with constant rate
vectors is that long vectors are displayed at a faster writ-
ing speed than short vectors; the intensity of the CRT beam
must therefore be adjusted to be proportional to vector
length. The problem with constant rate vectors is that the
necessary hardware is incredibly complex, and would be pro-
hibitive for this application. Therefore, constant time
vectors will be used. The intensity problem is simplified
by the fact that the ratio of the length of long vectors to
short vectors is small (5 or 10:1), and by the fact that the
intensity control is not very critical.

There are two methods of generating constant time vectors:
the RC method and the integrator method. In the RC method,
the absolute X and Y positions of the vectors are stored in
ROM. The ROM drives two D/A converters generating X and Y
voltages. The output of the D/A converters is the addresses

of the X and Y positions. These points are connected by
sending the D/A voltages through RC low pass filters, caus-
ing the beam to approach the vector end points exponen-
tially. If the X-RC and the Y-RC time constants are iden-
tical, straight lines are formed between points. In order
to compensate for the variation in speed across the CRT face
the Z circuit must be fed through an RC high pass circuit.
The amplitude of the Z-RC waveform must be proportional to
vector length, which is equal to the square root of the sum
of the change in X squared plus the change in Y squared
(Pythagorean theorem). The delta X and delta Y values must
be generated with two analog delays (S/H) and subtractors, or
two digital delays (latches) and subtractors, or with addi-
tional ROM to store the Z value. This additional hardware
is not required with the integration method.

In the integration method, the delta X and delta Y values
of a segment are stored in the ROM instead of the absolute
X and Y postitions. These values are converted to bipolar
analog currents by driving the four MSBs of two D/A converters
By integrating a delta X current value for a constant time,
the beam moves linearly an amount equal to delta X. This
method has the advantage that the delta X and delta Y values
do not need to be derived in order to calculate a z value.
The resolution of delta X and delta Y values to generate
high quality stroke characters is only three bits magnitude
plus one bit sign. If stored in ROM as two four bit offset
binary values, the total ROM requirement could be met with
one 256 by 8 bit part. This would be a good low cost, low
power organization (see figure D-E).

The D/As will require output offsetting to generate bipolar
currents. The intensity circuit must generate the square
root of the sum of delta X squared plus delta Y squared.
Since only low precision is required, this function can be
approximated as follows. Start with two four bit offset
binary values (delta X and delta Y). Then assume that the
least significant bit is not required, and that the magnitude
information in the middle two bits is sufficient. Then de-
termine the absolute value of the middle two bits by exclu-
sive ORing them with the sign bit. This value will have an
error of +0 or -1. This reduces the data to four bits, two
delta X bits and two delta Y bits. The vector length cal-
culation and analog conversion can now be done with sixteen
or less resistor values and a 16 to 1 analog multiplexer.
The multiplexer's select inputs are these four bits; its

analog inputs are the sixteen resistors which have a common reference voltage. The multiplexers' output drives the summing junction of an op-amp. The parts cost for this circuit is less than the cost for additional ROM to store the intensity value for each vector.

One problem with the integrator method is that the integrators tend to accumulate any input offset errors, causing inaccuracies in the beam positioning. The D/A output current for a digital input of offset binary "0" must be set accurately to reduce this to an acceptable level. This can be done by using two precision tracking resistors, one for the D/A reference current input and one from the D/A reference voltage to the integrator summing junction. The zero accuracy will then depend only on the resistor match.

A positioning circuit will provide X and Y voltages for the lower left corner of each character. The Y voltage is constant for all characters, and the X voltage varies for each character. The X voltage generator will consist of a 16 input analog MUX and a resistor ladder. The character select code will be used to select a tap of the ladder via the multiplexer. In this way, character spacing will be determined by resistor values and changes in character spacing (for the inclusion of a decimal point for temperature display) can be implemented with resistors and analog switches. The character position logic will also reset the integrators at the beginning of each character so that errors will not accumulate during the display of 16 characters. The first delta X and delta Y value of each character will move the CRT beam from the lower left corner of the character to the starting point of the character. This segment will be blanked for all characters.

The voltages from the integrators will be scaled down to the proper character size on the CRT and added to the character positioning voltages to generate the X and Y control signals.

4.4 CRT Driver Circuitry

The CRT used in the 503/504 is an Amperex Type 55261 post deflection amplifier (PDA), electrostatic deflection, low power CRT. This CRT is a good choice for the 505/506 as well, since the brightness, efficiency and size requirements are about the same as the 503/504. One alternative that will be considered is to use the Amperex Type D14-251 CRT. This tube is a monaccelerator design, and although less bright, uses lower acceleration potential (2KV instead of 4KV) reducing power dissipation, and simplifying the high voltage circuitry. Some of the brightness lost will be regained by using a more optimum CRT filter. Experiments will be performed during Phase II to determine if the D14-251 tube can provide adequate brightness. The non PDA is preferred since it simplifies the high voltage power supply and costs $30.00 less than the PDA tube.

4.41 Power Supplies

The required power supply voltages for the electronic circuitry were defined in section 3.36 as +5.0V and +10.0V. The remaining voltages are completely dependent upon CRT choice, but assuming that one of the two previously mentioned Amperex devices is used, these voltages can be coarsely defined.

Electrostatic deflection tubes have very narrow constraints concerning the bias voltages that must be applied. The cathode (K), control grid (gl) and heater must be biased at -2KV with respect to the PDA electrode in the 55261 PDA tube or with respect to the accelerator in the D14-251 tube. The deflection plates must be biased near the PDA electrode or the accelerator. This means that the X and Y control voltages of the tube must be biased +2KV with respect to the Z control (K, gl). Therefore both circuits cannot be grounded; one must be biased at high voltage. Since the low level control voltages are all referenced to ground, some means must be provided to couple either the X and Y, or the Z control signals to high voltage bias levels. The X and Y voltages must be dc coupled, accurate, and stable; they would be the most difficult to bias at high voltage. The Z signal however is less precise, and would be easier to ac couple. The Z signal could be coupled to -2KV bias with an ac coupling capacitor, and dc restored with passive components. This requires that the Z signal have a well defined blanking level that can easily be clamped, but this should not be a problem. This technique is commonly used in television monitors, and is used in the 503/504.

If the 55261 is used, a total of 4KV is required between the cathode and the final accelerator. This will be accomplished as follows: cathode control grid and heater at -2KV; PDA electrode, deflection amplifiers, and astigmatism control near zero; and the final accelerator at +2KV. If the D14-251 is used, the biasing will be the same except that the PDA electrode will be replaced by the final accelerator, and the +2KV supply can be eliminated.

The controls for the CRT are focus, intensity, and astigmatism. The focus grid is biased near the cathode, and will float at high voltage (-1.8KV). The astigmatism control is biased near ground and can operate from a deflection supply (100 volts). The intensity control will actually require two components: one to bias the tube at the optimum operating point, and the other to modulate the gain of the Z signal. The bias control can be designed to float at -2KV or it can be biased near ground with additional circuitry. This potentiometer is adjusted only once during manufacturing to compensate for tube-to-tube variations. The gain poteniometer will be labeled "Intensity" and will be user accessible for brightness control. This poteniometer will be biased near ground.

The bias placement can affect the safety of the operator. The required adjustment range of the pots allows the use of small inexpensive trimmers, but if a trimmer is floating at high voltage, there is a chance that arcover to the users adjustment tool could occur. The astigmatism, focus, and CRT bias pots will be accessible by cover removal only, so safety is less of a problem, but should still be considered.

The deflection amplifier supply voltages are also dependent on CRT choice since the two CRTs have different deflection sensitivities. If the 55261 is selected, the supplies will be +85V for the Y amplifier and +170V for the X amplifier. If the D14-251 is selected, the supplies will be 120V for the Y amplifier and 240 volts for the X amplifier. The Z amplifier will operate from the lower of the two voltages.

The multiple output switching regulator approach discussed in section 3.36 will be used to generate all of the power supply voltages. The $\pm$10.0V, +5.0V, +85V and +170V supplies will be generated with transformer windings, full wave rectifiers, and filters. These voltages are all within the capability of conventional enamel insulated wire. The two windings that require special precautions are the high voltage winding and the heater winding. The high voltage winding

will feed a voltage quadrupler to minimize the voltage at
the transformer and to eliminate the capacitive and resonant
effects of high turns windings. The voltage at this winding
can therefore be limited to 500V peak. With careful winding
techniques enamel wire can also be used for this winding.
Since it must float at -2KVdc, the heater winding presents
some special problems. Fortunately, the voltage is only 6.3
volts, therefore very few turns are required. This winding
will be wound with high voltage insulated wire, and will be
insulated from the core and the other windings.

The control for the power supply will be implemented with a
standard pulse width modulator IC driving two push-pull
switching transistors. Feedback for the regulator will be
derived from the +10.0V supply, and an adjustment will be
provided to set this voltage precisely.

There will be several high voltage wires connecting the power
circuitry, and the CRT. There will also be large power supply
components mounted on the power circuit board; it is there-
fore desirable to use a power supply assembly that is separate
from the main electronics card cage. The assembly will con-
sist of a printed circuit card for mounting all components,
and a transformer/high voltage subassembly will contain all
circuitry with greater than 250 volt potentials. The material
for the assembly enclosure will be vacuum formed plastic if
shielding is not required, or mu-metal or steel if shielding
is required. Access holes will be provided for high voltage
adjustments.

4.42 Deflection Amplifiers

The deflection amplifiers provide high voltage signals to the
CRT X and Y deflection plates. Their inputs are $\pm5V$ signals
from the CRT control switching circuitry (section 4.319).
The CRT deflection sensitivities are 19 V/cm for X and
9.5V/cm for Y for the 55261 CRT, and 23V/cm for X and 13.5V/cm
for Y for the D14-251 CRT. The required full scale deflection
voltages are therefore between 190V and 230V for X, and 95V
and 135V for Y. These amplifiers must be dc coupled through-
out. There are four basic configurations for the amplifiers.
They are:

1) Single output amplifier with single supply driving
   one plate with the other plate dc biased to ½ the
   supply voltage
2) Single output amplifier with two supplies driving
   one plate with the other plate grounded.

3)   Differential output amplifier with single supply
      driving both plates; output biased to ½ the supply
      voltage.

4)   Differential output amplifier with two supplies
      and the output biased to ground.

Since the maximum output voltage could be as high as 230
volts p-p, a single ended amplifier would require compli-
mentary 300V bipolar transistors. PNP transistors of this
voltage are both slow and expensive. In addition, the
power dissipation of this amplifier would be higher than
that of two lower voltage differential output amplifiers
since the voltage swings are greater.   Therefore circuits
1) and 2) will not be considered. Since there is no advan-
tage to biasing the plates to ground, and circuit 4) requires
extra power supplies, circuit 3 will be used: the amplifiers
will have differential outputs and will be biased at ½ the
supply voltage.

The actual design of the circuit will be based on a high
speed, low power video amplifier design (see figure D-D).
The amplifier consists of complimentary common emitter stages
with their collectors tied together at the output. The PNP
device pulls the output to the positive supply and the NPN
device pulls the output to ground. The amplifier does not
supply any dc output current except to drive the feedback
network. The drive for the PNP output transistors is cap-
acitively coupled, and the drive to the NPN transistor is
dc coupled to a single drive source. A low voltage compli-
mentary emitter follower stage is used as the drive source,
providing low drive impedance and high speed. The amplifier
configuration is inverting, and feedback will be applied to
linearize the gain. Because the amplifier uses negligible
quiescent current efficiency is very good.

There are several adjustments required for the deflection
amplifiers. Gain and offset controls are required to com-
pensate for CRT unit-to-unit variations. In addition, some
means of rotating the CRT trace must be provided. A rotation
coil is provided, but since this coil can consume as much
as 360mW of power, it will not be used. The low power
solution to this problem is to add an adjustable amount of
vertical deflection voltage to the horizontal signal and
an adjustable amount of horizontal voltage to the vertical
deflection signal. The first control adjusts vertical tilt,
and the second control adjusts horizontal tilt, resulting
in trace rotation. This approach is used in the 503/504.

4.43 Video Amplifier

The video amplifier combines the blanking logic signal and
the analog intensity signal into one video signal which is
amplified and applied to the CRT control grid. The ampli-
fier's linearity is not critical, so an open loop transistor
stage will be used. The stage will be a cascode amplifier
with the blanking signal and the intensity control signal
both injecting current into the output transistor stage.
The power supply for this amplifier will be the lower of
the two deflection amplifier power supplies.

4.5 Battery/AC Power

The battery provides dc to the monitor's power supply cir-
cuits when ac is not available. When ac is available, the
ac is converted to unregulated dc, which charges the battery
through a trickle charging circuit, and provides power to
the monitor's power supply circuits.

4.51 Battery and Charger

Corometrics has expressed an interest in using the 503/504
battery for the 505/506. Since this battery is a good quality,
standard NiCad battery and its size and power capability are
suitable for the 505/506 requirements, we concur with its use.
Corometrics has had no reliability or other technical problems
with the battery.

A discrete constant current regulator will provide 150mA of
trickle from the unregulated dc supply. This will fully
charge a dead battery in fourteen hours.

4.52 Unregulated DC

Unregulated dc will be generated in a conventional manner
using 50-60Hz transformer, full wave rectifier, and filter
capacitor. An approach was considered which would eliminate
the filter capacitor using the battery to provide the energy
storage. Several problems make this method less desirable
however. One problem is that with a completely dead or de-
fective battery the monitor will not operate, since the in-
put voltage to the regulator circuitry would be too low.
Also, the charger circuitry is considerably more complex
for this approach since it must monitor the current draw of
the monitor and adjust the battery input current to be equal
to the monitor current plus the charging current. In addition,
the circuit would operate from unfiltered dc making it sus-
ceptable to line transients. Considering these problems and
the fact that there is adequate room in the monitor for a
filter capacitor, the conventional approach will be used.

4.53 Battery Low Indicator

A battery low LED on the front panel will indicate when approx-
imately ½ hour of operation is left in the battery. The cir-
cuit will be comprised of a comparator with one input connected
to the battery voltage through a voltage divider. Hysterisis

will prevent output oscillations. The comparator will drive
an LED directly through a current limiting resistor. The
comparator threshold voltage will be determined empirically
using several batteries.

5.0 Product Conclusions

Concluding Phase I we feel confident that the goals that were established for the 505/506 are realizable to your satisfaction. The design goals other than the specifications that pertain to conclusions of the conceptual development of the monitor will be discussed in this section. These relate to the mechanical and packaging requirements, the product factory cost, and the important power dissipation requirement that affects all engineering decisions.

It is very difficult to produce exact quantities for these conclusions without actually designing, building, and measuring the proposed 505/506. Since the 503/504 is an actual, successful product which is conceptually very similar to the proposed 505/506, the product conclusions will be stated as a function of the parameters of the 503/504.

5.1 Cost

The factory cost of the 505/506 will be slightly higher than that of the 503/504. Some of the functions will be simplified or redesigned with more recent technology, with a resultant cost savings, but several additional functions will be added that will probably outweigh the savings. The poor serviceability of the 503/504 will be eliminated, but it will be at the cost of more elaborate PC board mounting. Some of the proposed power saving schemes, necessitated by additional circuitry and no increase in power consumption, will add to the cost slightly. Based on our present judgement, we expect the factory cost of the electronics of the 505/506 to increase by less than 20% compared to the 503/504 costs.

We feel that this is justifiable, considering the extent of improvements that **will be incorporated** in the new monitor.

5.2 Power

Based on a required four hour battery operation time, compared to three and one half for the 503/504, the power dissipation requirement for the 505/506 is slightly lower. The amount of electronics, however, will increase because of added functions. Hence that power dissipation must be lower on a per function basis. This requirement will be met by using newer technology, low power parts wherever possible. The op-amps and comparators used in the 505/506 will consume a total of approximately 0.75 watts less than those in the

503/504. The 16K dynamic RAM will use approximately 0.25 watts less than the sixteen 1K shift registers of the 503/504. These two changes total 1.0 watt savings alone, enough to power all the additional features of the 505/506. Other areas where power savings may be realized are in the pressure transducer drive and in the power supply efficiency. If it is decided to use a lower brightness CRT, this will also save power.

We presently feel confident that the power dissipation requirements of the 505/506 can be met.

5.3 Board Area/Partitioning

One of the design goals of the 505/506 is to maintain the compact size of the 503/504 while improving serviceability. We have been involved in the decisions concerning internal packaging, and feel confident in the approach that Corometrics has chosen to attain this goal. The circuit technology that will be used in the 505/506 will be very similar to that of the 503/504. This means that on a function per function basis, board areas will be about the same. However, as there are slightly more functions in the 505/506, more board area will be required. The precise amount can only be determined after a detained circuit design, but we presently feel confident that our original estimate of 10% to 20% more board area than the 503/504 can be maintained. This corresponds to a total area of between 340 and 370 sq.in. Corometrics' mechanical engineers have selected a card cage approach to packaging the bulk of the electronic circuitry, with special assemblies for the high voltage power supply, and front panel controls. This approach seems quite efficient in terms of volume usage, and is good design in terms of consistency of board sizes, interconnections, and serviceability. The remaining components (power transformer, high, and low voltage power assemblies and battery) are located around the neck of the CRT. Other than possible transformer hum pickup problems, which can be resolved by shielding, this also seems like a very efficient approach.

Currently, there are six circuit boards proposed for the 505/506 card cage. The front end circuitry will be located on the board closest to the right hand side of the case. This will provide a convenient and direct place to mount the patient connectors. The board farthest to the left will be used for the X, Y, and Z amplifiers, since they will require special cables to connect them to the deflection plates

of the CRT. Connectors will be provided at the top of the board for this function. With the patient connections and the front end input circuitry on the right-most board and the CRT drive circuitry on the left-most board, the logical signal flow is from right to left with the display control boards towards the left and the physiological processing boards towards the right. Other than this rule of thumb, there are few other constraints on the partitioning of the circuits. Individual functions should be kept on a single board, but since most functions have very few input and output connections, the number of board interconnects is low and the partitioning requirements are quite loose.

6.0 PHASE II DISCUSSION

6.1 Task Partitioning: Octek/Corometrics

Octek's primary responsibility for Phase II is the design
and construction of a prototype model of the 506 monitor.
Associated with this are a number of related tasks: PC lay-
out, mechanical layout, testing (including environmental and
safety testing), documentation, etc. Since Corometrics has
the facilities and manpower to assist with some of these tasks,
and because Corometrics will be responsible for taking the
design from the prototype stage into production, it is bene-
ficial for both parties that Corometrics assist or perform
some of these tasks.

Octek's responsibilities will be limited in the following
areas:

PC layout - Corometrics will be responsible for the layout
            of all PC boards. Octek will assist Corometrics
            draftsmen to provide initial inputs as to any
            specific requirements of sensitive circuits.
            Octek will also resolve any layout problems and
            will provide final review and acceptance of lay-
            outs prior to etching the boards.

Fabrication -
            All PC boards will be fabricated by Corometrics.

Mechanical Layout -
            All mechanical layout is presently, and will con-
            tinue to be the responsibility of Corometrics.
            Octek will provide direction where necessary if
            circuit performance will be affected.

Mechanical Construction -
            Corometrics will Provide Octek with a mechanical
            prototype.

All of the above items can have a serious impact on the sched-
uled delivery of a final prototype. Our proposed schedule
assumes a rapid turnaround time by Corometrics with respect
to the above tasks.

Although the actual functioning prototype capable of meeting
all of the performance and functional specifications of Appen-
dices A and B is the primary output of Phase II, there are
several other items that need to be defined more accurately,

such as documentation. Octek will provide a complete docu-
mentation package with the prototype which will include:

-A complete set of schematics for each board or module.
-Parts list for each board or module.
-A brief theory of operation for each section.
-Design notes.
-Test Data (ambient conditions).

Corometrics draftsmen may assist with the drawings of the
schematics.

Another area of joint responsibility is final testing. Octek
will design all circuits with environmental constraints con-
sidered, particularly temperature. However, with the excep-
tion of temperature evaluation of critical circuits at the
breadboard stage, Octek will not be responsible for any en-
vironmental testing. Phase III of this project will be to
assist Corometrics in getting the design into production.
Any environmental problems will be solved in Phase III.

Octek will test for patient leakage, electrostatic discharge,
and overload protection. However, all other safety tests
will be the responsibility of Corometrics. Corometrics
will loan or provide Octek access to any special test equip-
ment that may be required for the design and test of the
505/506.

6.2 SCOPE

The scope of Phase II is to design, build, and test a working
prototype of the 506 neonatal monitor that will meet all of
the specifications of Appendices A & B. The previous Section
(6.1) delineates some of the shared responsibility of this
task. Octek will submit a final test plan to Corometrics
prior to final delivery. Following acceptance of the test
plan and completion of the prototype, Corometrics will wit-
ness the successful testing of the 506 prototype at Octek,
and accept delivery of the unit, documentation and test data.
This will conclude Phase II.

6.3 COST AND DURATION

The cost of Phase II to Corometrics shall not exceed $207,000.
Such sum includes all professional services, materials and
other expenses to be incurred by Octek on behalf of Coro-
metrics during this period. Professional services shall
be charged Corometrics at Octek's standard rates at the
time the professional services are performed.

Although Octek feels the proposed time and costs are adequate
to bring the program to a successful conclusion, changes in
the direction of the work, dictated by Corometrics in writing,
which are contrary to those set forth herein, may require
extension of the time limits and increased expenditures for
completion. Octek will bring to Corometrics' attention as
soon as recognized, any factors which will affect cost or
time limits.

Upon the execution of this agreement by Octek, Corometrics
shall pay to Octek the sum of $20,700. Upon the commence-
ment of work, Octek will submit invoices to Corometrics on
a monthly basis. Such invoices will conform to Octek's
standard invoice procedures and will list separate figures
for professional services.

The $20,700 advance payment will be credited towards the
first invoice or invoices until such sum has been expended.
Corometrics will pay the balance due and owing under the
invoices within 15 days of receipt.

The duration of Phase II shall be a maximum of 7.0 months
Work will commence immediately with execution of this agree-
ment.

All of the terms of Phase I concerning confidential, third
party, and patent information remain in effect through
completion of Phase II.

APPENDIX A

FUNCTIONAL SPECIFICATIONS

1.1 ECG Amplifier Functional Characteristics

The ECG amplifier is an isolated amplifier which feeds the upper solid trace display, digital heart rate meter, and system connector. It contains the following features:

1. Two lead operation - requires that two leads only be attached to the patient instead of the usual three leads.

2. Slew rate limit - limits the slew rate and therefore the amplitude of pace pulses so that they will not trigger the heart rate meter. Only the heart rate detector is slew rate limited so that pacer display is not affected.

3. Fast recover circuit - returns the ECG to on screen limits within 0.5 to 2 seconds after defibrillation, bovie, or other overload.

4. Manual gain control - The amplitude of the trace on the screen can be set manually. The QRS detect circuit will operate off the X1000 ECG or similar signal (before the adjustable gain stage.)

1.2 Pressure Amplifier Functional Characteristics (506 only)

The pressure amplifier is an isolated amplifier which feeds the lower solid trace display, digital systolic, diastolic and mean meters, and the systems connector. The pressure waveform is displayed and its amplitude is controlled by the pressure gain control which is calibrated at 75mm and 150mm positions. If the pressure exceeds a fixed limit of approximately 300mmHg, or if mean pressure increases to 10mmHg and then drops below 5mmHg, an alarm sounds at full volume.

1.3 Respiration Amplifier Functional Characteristics

The respiration amplifier is an isolated amplifier which feeds the lower solid trace display, digital respiration rate meter and the systems connector. The respiration waveform is displayed and its amplitude can be set manually. The respiration detection circuit will have both a fixed (manual) and tracking (auto) threshold controlled by a front panel switch.

1.4   Temperature Amplifier Characteristics

The temperature amplifiers are isolated amplifiers which feed the digital temperature meter(s).

1.5   Digital Display Meters

Heart rate, systolic pressure, diastolic pressure, respiration rate and either mean pressure, temperature 1 or temperature 2 are displayed digitally at the top of the CRT on the 506. Heart rate, respiration rate, temperature 1 and temperature 2 are displayed digitally on the 505 CRT. When the heart rate exceeds a limit for more than three seconds, the digital display of heart rate blinks and an audible alarm is sounded. When apnea exceeds the preset apnea alarm delay period, or respiration rate exceeds the maximum limit, the digital display of respiration rate blinks and an audible alarm is sounded. Displays are updated every two seconds. The minimum input at the front end for reliable QRS detection is 0.25mV p-p; maximum input is 5mV.   Detection of a QRS complex will cause an audible beep if the side panel volume control is turned up. In the "manual" mode the threshold of respiration detection is equivalent to 6mm on the scope display. In the "auto" mode the threshold will track the respiration signal. Respiration gain is controlled by the front panel RESP GAIN potentiometer. Detection of a breath causes a green RESP light to illuminate.

1.6   Solid Trace Display Functional Characteristics

The top solid trace display shows the last 4 seconds of the ECG waveform or the last 3-1/3 minutes of heart rate (HR). The bottom trace shows the pressure or respiration waveform. 4 seconds in ECG mode and 3-1/3 minutes in HR mode. When the freeze button is depressed, both traces are frozen for review.

1.7   Operator Controls

1.7.1   Heart Rate Alarm Limits

A dual indicating slide potentiometer used for setting the low and high heart rate limits. The low heart rate limit can be set between 40 BPM and 200 BPM. The high heart rate limit can be set between 80 and 240 BPM.

1.7.2 Apnea Limit

A four position slide switch used for setting the apnea period to Off, 10, 15, or 20 seconds. The apnea alarm also acts as a low respiration rate alarm, i.e. the respiration timer is not reset with every breath, rather 4 seconds are subtracted from it for each breath. The apnea timer limit is 6 to 8 seconds longer than the apnea period.

1.7.3 Respiration Rate Limit

An indicating slide potentiometer used for setting the high respiratory rate limit between 40 and 120 BPM.

1.7.4 Digital Display Select

A three position rotary switch used for selecting mean pressure, temperature 1 and temperature 2 for readout on the right-most digital display.

1.7.5 ECG Gain

A potentiometer used for setting the gain of the ECG amplifier. Gain may be varied from X300 to X5000. At center position, the gain is approximately X1000. Fully CCW is the "AUTO" position where gain is set automatically by the monitor. The auto gain range is the same as the manual gain range. Pressing the control injects a 1mV square wave into the ECG signal.

1.7.6 Respiration Gain

A potentiometer used for setting the gain of the respiration channel. The respiration gain may be varied over a 15 to 1 range.
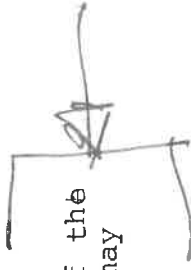
1.7.7 Pressure Gain (506 only)

A two position rotary switch used for setting the pressure gain. In the "50" position, the gain on the screen is 50mmHg for 5 cm deflection. In the "125" position the gain on the screen is 125mmHg for 5 cm deflection. Pressing the control zeroes the pressure signal.

1.7.8 Display

A latching pushbutton which turns power on to the
monitor. The battery charges operates independently
of this control and operates whenever the monitor
is plugged in.

1.7.9 Freeze

A latching pushbutton which stops or "freezes" the
moving solid trace display when pushed.

1.7.10 ECG/HR

A latching pushbutton which selects either ECG at
25mm/sec or HR at 3cm/min for the top trace.

1.7.11 RESP/PRES(9506 only)

A latching pushbutton which selects either respira-
tion or pressure for display on the lower trace.

1.7.12 Alarm OFF

A momentary pushbutton which disables the audio
alarm for two minutes when pushed. A LED flashes
when the audio alarm is disabled. Pushing the button
again re-enables the audio alarm.

1.7.13 Alarm Volume

A potentiometer on the side panel used for setting
the volume of the alarm tone. In the fully CCW
position the alarm is turned off and the alarm
off LED flashes.

1.7.14 Beep Volume

A potentiometer on the side panel used for setting
the volume of the QRS beep. In the fully CCW posi-
tion the beep is turned off.

1.8 User Accessable Internal Controls

   1.8.1 Intensity

   1.8.2 Focus

   1.8.3 Astigmatism

1.9   Indicators

   1.9.1.   Digital Display

        A digital display which writes numeric characters
        at the top of the CRT. From left to right the
        display reads: Heart Rate, Resp. Rate, Systolic
        Pressure, Diastolic Pressure, Selected Parameter
        on the 506, and beart Rate, Respiratory Rate,
        T1 and T2 on the 505.

   1.9.2   Leads OFF Light

        A red LED which flashes when the impedance between
        the electrodes is too high for proper operation.

   1.9.3   QRS Light

        A yellow LED which flashes every time a QRS complex
        is detected.

   1.9.4   Respiration Light

        A green LED which illuminates coincident with the
        detection of each inspiration.

   1.9.5   Line Light

        A green LED which lights whenever the unit is plugged
        in, regardless of whether display is on or off.

   1.9.6   Low Battery Light

        A red LED which flashes when the battery has a minimum
        of 1/2 hour of charge left, regardless of whether
        display is on or off. The low battery indicator
        will flash once when power is turned on to verify
        that it is operational.

   1.9.7   QRS Tone

        An audible tone which is produced every time a QRS
        complex is detected. Volume is dependent on the rear
        panel beep volume control. In the fully CCW position,
        the control turns the beep off.

   1.9.8   Alarm Tone

        An audible tone produced whenever an alarm condition
        exists and the alarm is not turned off. Volume is
        set by the rear panel alarm volume control. In the

fully CCW position, the control turns the alarm
tone off.

1.10 Side Panel Connectors

1.10.1 Isolated ECG Input Connector

5 pin MS series connector located on side panel
for connection to patient cable.

PIN A - Right arm
PIN B - Left Arm
PIN E - Shield

1.10.2 Isolated Pressure Input Connector

Lemo connector

1.10.3 Isolated Thermistor Input Connector

Two miniature phone jack connectors for connection
to thermistors.

1.11 Rear Panel Connectors

1.11.1 System Connector

24 pin Amphenol "Micro Ribbon" series connector
with the following signals brought out:

ECG
B-B Heart Rate (V = (BBHR - 135)/30)
Pressure   (V = (5*P)/Range -2.5)
Respiration
Temperature 1
Temperature 2
Channel 2 Waveform (Pres. or Resp.)
Signal Ground
Alarm
Chassis Ground
Alphanumerics (Format includes BCD data, clock, reset)

1.11.2 Sync Connector

Three wire phone jack located on the rear panel
provides ECG output for connection to external
Recorder or Defibrillator:

Tip - ECG Out
Ring - Signal Ground
Sleeve - Chassis Ground

APPENDIX B

PERFORMANCE SPECIFICATIONS

2.1 ECG Amplifier

*Frequency Response: .05 to 50Hz, +5, -3dB to
                                scope display at 1mV p-p
                                input level

                                .05 to 100Hz, +0, -3dB to
                                rear connector at 1mV p-p
                                input level.

Common Mode Rejection   100dB at 50 to 60Hz with 5K
                                source imbalance.

*Gain   Adjustable X300 to X5000;
                                X1000, at nominal gain
                                position. Manual gain con-
                                trol provided.

Input Impedance: 10 megohms differential dc
                                to 100Hz.

Input Offset Tolerance: +300mV.

*Noise   5uV rms referred to input at
                                ECG output dc to 100Hz.

Common Mode Input Impedance: 12 megohms from patient leads
                                to chassis ground dc to 60Hz.

Defibrillator Protection: Will withstand 15 Low pulses
                                at 20 second intervals
                                from defibrillator set to
                                400 WS stored energy and
                                delivered across a 200 ohm
                                load in parallel with the
                                two input leads.

*Reset Recovery: Automatic return to baseline
                                on screen 0.5 to 2.0 seconds
                                after an electrosurgical or
                                defibrillator overload.

Output: High level single ended
                                ECG output.

                                On rear panel. Output level
                                dependent on gain setting.
                                1V/mV at X1000 gain setting.

*Calibration Signal: 1mV +2.5% referred to
                         input.

Output Impedance: < 120 ohms.

*Output Dynamic Range: +3.5 volts

*Output Offset: <50mV for dc input at
                         nominal gain.

Output Current: +5mA.

2.2   Pressure Amplifier

*Frequency Response: dc to 40Hz, +0, -3dB.

* Gain with 5uV/V/mmHg sensitivity transducer

Range: -10 to 75mmHg in "75"
                         gain position.
                         -30 to 150mmHg in "150"
                         gain position.

Scope: 5cm/75mmHg +5% in "75"
                         gain position.
                         5cm/150mmHg +5% in "150"
                         gain position.

Output Connector: 1V/15mmHg +2% in "75"
                         gain position.
                         1V/30mmHg +2% in "150"
                         gain position.
                         Output voltages are
                         offset 1/2 of full scale.

*Zero: zero reference line on
                         the CRT screen within +2mm.
                         Digital display within +1mmHg.
                         Output within +2mmHg.

*Noise   0.5mmHg p-p.

Common Mode Input   > 12 megohm from patient
Impedance: leads to chassis ground dc
                         to 60Hz.

*Output: Common mode signal output on
                         rear panel. Output level

.

dependent on gain control.
Output zero offset 1mmHg
referred to the digital
display.

*Zero Adjustment Range: > +100mmHg

*Zero Drift: .25mmHg/°C excluding trans-
                            ducer.

Output Impedance: < 120 ohm

2.3 Respiration Amplifier

Frequency Response: .1 to 5Hz, +0, -3dB to
                            scope display and rear
                            connector at 1V p-p out-
                            put level.

Gain: 1.0 +10% volts/ohm to
                            +RESP output on rear
                            connectors.

                            Adjustable to RESP out-
                            put from -0.5V/ohm to
                            -4.5V/ohm.

                            Adjustable to scope dis-
                            play, from .05cm/ohm to
                            4.5cm/ohm.

Total Electrode and
Cable Impedance: 0- 4K ohms.

Carrier Frequency: 20KHz +25%

Respiration Measuring
Current - (measured with
AAMI load):   200uA max.

Noise: < 10 milliohms rms referred
                            to input, 1-100Hz.

Common Mode Input
Impedance: >12 megohms from patient
                            leads to chassis ground dc
                            to 60Hz .

Range: 0-150 BPM.

Adjust by servo control

Output:

Signal output on rear panel. Output level dependent on gain setting. See gain spec.

Output Reset:

Reset prevents the RESP output from exceeding ± 4 volts.

Output Dynamic Range

$\pm 3V$ minimum.

Output Current:

$> \pm 5mA.$

Output Impedance:

$< 120\Omega$

Output Offset:

$< \pm 1200mV$

Defibrillator Protection:

Will withstand 15 Lown pulses at 20 second intervals from defibrillator set to 490 WS stored energy and delivered across a 200ohm load in parallel with any two input leads.

24. Digital Heart Rate Meter

*Range:

0 to 250 BPM

*Input:

0.25mV to 5.0mV p-p returned to the input.

*Threshold:

Equivalent to 0.15mV referred to input.

Triggers on R-waves of either positive or negative polarity.

*Accuracy:

3BPM or 5% of display whichever is greater above 30 BPM.

Response Time:

< 5 seconds for rates greater than 50 BPM and an input step change of 70 BPM.

*Low Alarm Limit Range:

40 to 200 $\pm$ 5 BPM

*High Alarm Limit Range:

80 to 240 ± 5 BPM.

Resolution:

1 BPM.

Alarm Setting Accuracy:

Better than ± 5 BPM.

*Alarm Delay: 3 seconds, -1, +2 seconds.

*Pacer Artifact Rejection: Slew rate limit of 0.2
                                 to 0.25mV/ms will prevent
                                 response to pacer spikes
                                 with proper electrode place-
                                 ment.

Update Rate: 2 seconds nominal

Resolution: 1 BPM.

2.5   Digital Pressure Meter

*Range: 0 to 150mmHg.

*Accuracy: +2mmHg or 3% of reading
                                 whichever is greater,excluding
                                 catheter artifact, with
                                 a recommended transducer
                                 properly zeroed.

*Zero: +1mmHg referred to rear
                                 connector.

Resulution: 1mmHg.

Update Rate: 2 seconds nominal.

2,6   Digital Respiration Meter

Range: 0 to 150 BPM.

Maximum Sensitivity: > 0.2 ohm at 1.4Hz.

Detector Response: The detector shall detect
                                 sine waves from 0.5Hz to
                                 2.5Hz at .5ohm.

Accuracy: +3 BPM or +5% of display
                                 whichever is greater above
                                 10 BPM. Below 10 BPM the
                                 rate fluctuates with each
                                 breath.

Response Time: 20 seconds plus the
                                 time to the next update
                                 for an input step change
                                 of 30 BPM.

Resolution: 1 BPM.

Threshold   manual-

                                 6mm referred to the CRT
                                 display auto-threshold
                                 will track the respira-
                                 tion signal.

Apnea Alarm Delay: 10 to 20 seconds.
                                 +3 seconds.

Update Rate: 2 seconds nominal.

2.7 Digital Temperature Meter

Range: 30°C to 45°C.
Accuracy: +0.2°C or better.
Response Time: Limited by Thermistor
                                 response time.
Resolution: 0.1°C
Update Rate: 2 seconds nominal.

2.8 Display

Total Viewing Area: 8x10cm.
                                 6.5x10cm available for
                                 ECG display.

*Pressure Analog Accuracy: +2mmHg or 5% or reading,
                                 whichever greater.

*Sweep Speed: 25mm/sec +5

Memory Time: 4 seconds visible on ECG
                                 3 1/3 min. on B-B Heart
                                 Beat.

Sample Rate: 240Hz. ECG equiv. for
                                 heart rate (~ 1K/screen)
                                 8 bit resolution.

Refresh Rate: 60Hz.

*Transient Response: <5% overshoot to step
                                 input of any magnitude
                                 up to full scale.

*Frequency Response: See Sec. 5.1 and 5.2

*Resolution: 8 bits.

Sampling Noise: <.3mm at any gain setting.

Horizontal Sweep Linearity: Better than 5% over full
                                    viewing area.

Phosphor Type: P31.

Brightness: Screwdriver adjustment

Vertical Linearity: Better than 5% from iso-
                                    lated inputs to scope dis-
                                    play.

Warm-up Time: 15 seconds.

Drift: Baseline shall not drift
                                    more than .5 cm within
                                    5 minutes after power
                                    turn-on.

2.9 Power Supply

Battery Type: NiCad.

*Battery Life: 4 hours.

*Low Battery Indicator: Indicates 1/2 to 1 hour
                                    of battery life left.

Charge Time: 14 hours to full charge.

Input Requirements: 100,110,117,127,VAC
                                    200,220,235,254 VAC
                                    +10% at 50 or 60Hz.

Power Consumption: 20 watts max.

*Hipot: > 2500 Vac rms 60Hz be-
                                    tween ac hot or neutral
                                    and green wire ground.

2.10 Physical Characteristics

Size: 6.0"H x 9.4"W x 14.4"D

Weight: 18 lbs. maximum

APPENDIX C

PATENT SUMMARY

3,545,429
"Respiration Monitor" 12/8/70, assigned to Becton Dickinson. This is an impedance pneumograph apparatus for monitoring and detecting apnea. The design is very outmoded.

3,587,562
"Physiological Monitoring System", 6/28/71, assigned to Becton Dickinson. This patent covers the technique used in the 503/504 whereby the floating power supply, respiration carrier, and ECG modulation all operate at the same frequency.

3,212,496
"Molecular Physiological Monitoring System" 10/19/65, assigned to United Aircraft Corp. This patent uses DC respiration excitation as part of a monitoring system that uses one amplifier to transmit ECG and respiration simultaneously.

3,948,250
"Physiological Information Display" 9/16/74, assigned to Becton Dickinson. This patent covers the seven segment display method used to display numerics on the 503/504 CRT.

3,532,087
"Respiration Rate Meter" 10/6/70, assigned to Hoffman-LaRoche, Inc. The design is an early respiration rate indicator using rate multiplication of the respiration wave.

4,000,401
"R-Wave Detector" 12/28/76, assigned to Tektronix. A method for detecting R-Waves by differentiating and then rectifying the ECG signal is presented.

3,465,103
"System for Combining Plural Isolated Physiological Signals Without Mutual Interference and With Reduced Noise Level" 6/23/66, assigned to United Aircraft Corp. The method used is to frequency modulate several physiological parameters on different carrier frequencies and then mix the modulated carriers onto a single isolation transformer.

4,191,195   "Coupling Circuit With Drive-Guard" 9/7/78, assigned to Hewlett Packard (Arthur Miller). This patent is for an ECG circuit which used an amplifier to drive the floating ground towards the common mode potential on the patients body, thus reducing common mode voltage.

4,200,109   "Coupling Circuit With Driven Guard" 9/7/78, assigned to Hewlett Packard (Richard McMorrow) This patent is similar to 4,191,195 except that in this configuration the floating amplifier drives the chassis ground. This circuit is particularly useful for neonatal monitoring as it uses only two leads.

3,988,690   "Amplifier Circuit Having a Floating Input Stage" 10/4/73, assigned to Tektronix Inc. This patent covers the use of a single transformer to transmit power to the floating circuitry and signal from the floating circuitry.

3,423,689   "Direct Current Amplifier" 1/21/69, assigned to Hewlett Packard (Arthur Miller). This is an isolated amplifier whose ground is driven by a grounded amplifier to eliminate common-mode signals.

3,915,154   "Method and Apparatus for Bio-Electrical Signal Measurement" 5/8/74, assigned to Hoffman-LaRoche Inc. This patent embodies an isolated ECG amplifier that is optically coupled and that used a patient connection to isolated ground to eliminate common mode signals.

3,444,856   "Blood Pressure Monitor" 6/24/1965, assigned to Morris Settler, This patent covers an electromechanical blood pressure indicator.

3,976,052   "Respiration Monitor" 1/10/75, assigned to Hewlett-Packard GmbH. This circuit is a respiration monitor that looks for cardiac coincidence and increases the respiration threshold level when coincidence is detected.
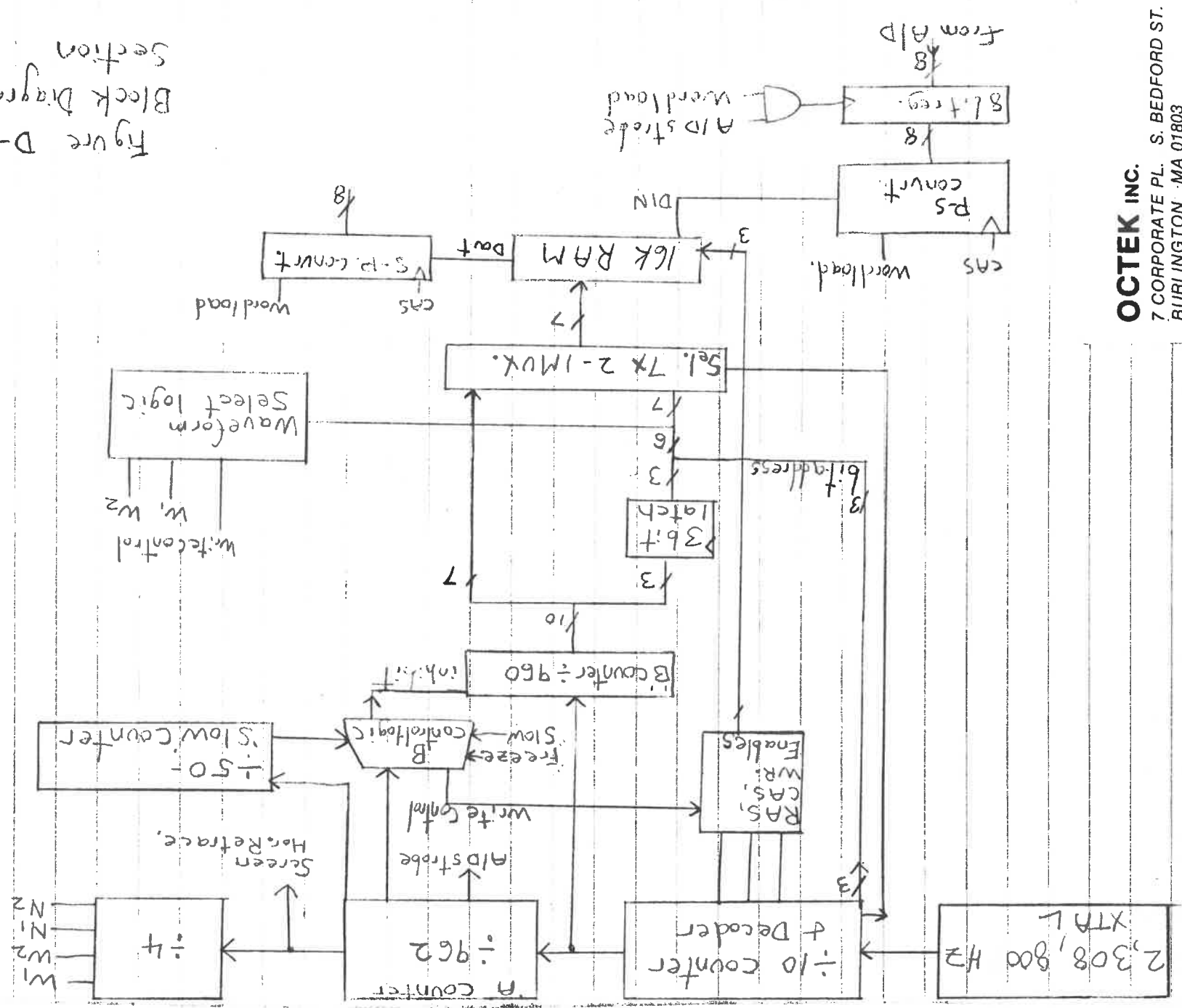
3,536,062   "Monitoring System for Heart Rate Respira-
              tion Rate and Blood Pressure" 3/30/67, assigned
              to Hoffman-LaRoche Inc. The system used an
              inflatable cuff to derive blood pressure and
              heartrate.

STROKE CHARACTER GENERATOR

Figure 3-1

mux 16:1

Z

Z0
Z1
Z2
Z3

RESET

Y

X

-SUM.

-INT.

Y.POS

D/A

D/A REF

Ros
Ros

ROM (256x8)

ΔX

ΔY

SIGN

LSB

SIGN

LSB

Z0 Z1

Z2 Z3

SEG.
CODE

CODE

CHAR.

FROM ROM RAM

X POSITION CODE