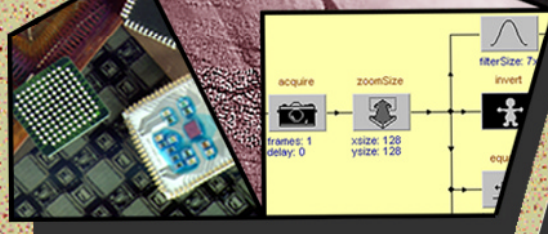


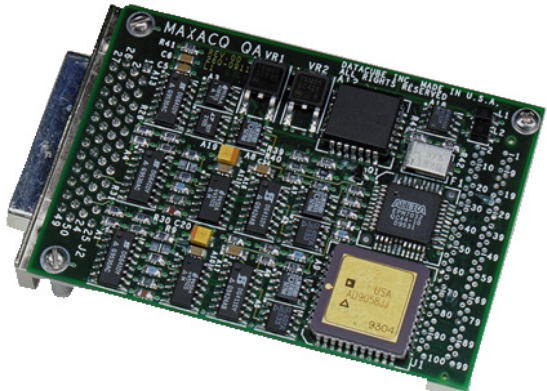


**Vision By
MaxPCI®**



QA MaxACQ Module

Dual 42MHz, 8-bit Analog Acquisition



- Video inputs for up to four cameras/sensors per converter (eight inputs total)
- 42 MHz, 16-bit FIFO capable of holding up to 300 K pixels
- Programmable gain, offset, and clamp
- Highly efficient noise isolated MaxACQ architecture
- Flexible sync selection and sync separation for composite video signals

MaxACQ Architecture

The QA module is one of the MaxACQ family of acquisition daughtercards from Datacube. The MaxACQ modules provide high throughput and simplify integration for a variety of cameras or sensors including area, line-scan, and TDI types, in a range of resolutions.

Under the [MaxACQ architecture](#), those functions such as timing control that are required by all types of acquisition (analog, digital, etc.) are handled by the image processing motherboard. This division of responsibilities results in individual acquisition modules that are smaller and less costly, with reduced noise.

Each of the MaxACQ modules uses a fine-pitch SCSI-style connector for easy integration. The use of an industry-standard connector cuts the cost and effort associated with building custom cables. Many of the required cables are available off the shelf, making the modules in the MaxACQ family more easily interchangeable.

Analog Acquisition

The QA acquisition module provides analog image acquisition for all boards that use the MaxACQ architecture. The QA module provides two independent 8-bit, 42 MHz A/D cameras that run synchronously. Because of the MaxACQ architecture's flexible timing design, timing can be derived from composite sync in the video (sync stripper, processor, and PLL), fed externally, or generated by the MaxACQ and fed to the cameras. Each A/D has a software configurable 4:1 frame rate video switch, programmable coupling, pre-gain offset, gain, and post gain offset, allowing for complete runtime configuration.

Features

- Dual 8-bit 42 MHz analog-to-digital (A/D) converters
- Programmable DC or AC coupling and DC restore
- Input video selector for up to eight cameras or sensors (4 per A/D)
- Flexible sync selection and sync separator for composite video sources
- EEPROM for ID, revision, and calibration data
- Completely jumperless configuration
- Acquisition on either one or two simultaneous, synchronous inputs
- Horizontal and vertical sizes of acquired image are independently programmable in increments of one from 4 to 16382 pixels
- Supports two synchronized sensors or a dual output multitap sensor
- 4:1 input multiplexers, one for each digitizer channel

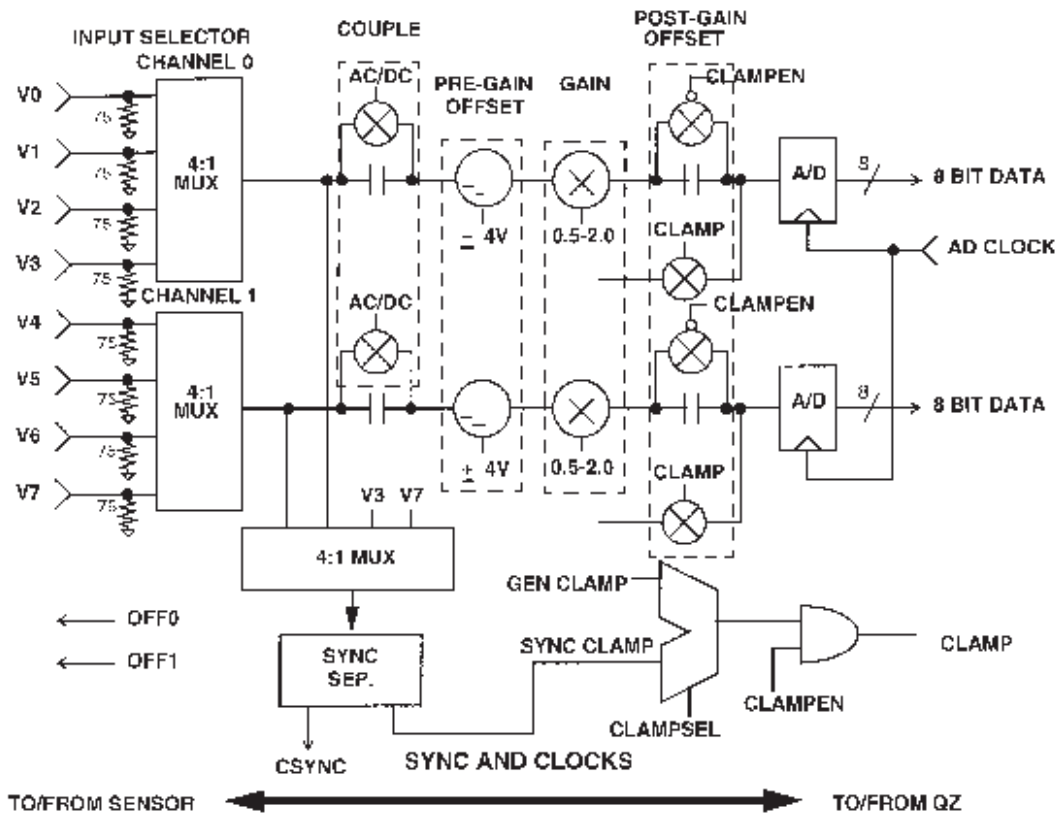
Specifications

Dual Analog-to-Digital Converters

- Dual programmable analog-to-digital (A/D) converters
- Clock rate from 100 KHz to 42 MHz
- A/D format: 8-bit, unsigned data
- A/D linearity: ± 0.5 LSB, no missing codes
- Low noise design:
 - Flat field design, 0.5 LSB or less of standard deviation; 3 LSB or less peak to peak noise
- Each A/D has its own:
 - 4:1 camera multiplexer
 - Channel 0 to select video inputs 0-3
 - Channel 1 to select video inputs 4-7
 - Programmable gain, offset, DC clamp

Input Data Buffer

- 42 MHz, 16-bit FIFO, capable of holding up to 300 K pixels, enables seamless processing of images in line-scan applications (continuous vertical)



Synchronization & Timing

- Flexible sync selection and sync separation (horizontal and vertical) for composite video sources
- Sensor timing interface with differential or single-ended inputs
- ADC clock from three possible sources:
 - External clock from scanner or cameras at 100 KHz to 42 MHz
 - Horizontal or composite sync from camera can be phase-locked to generate the ADC clock at 5 MHz to 42 MHz
 - Arbitrary clock can be synthesized at 100 KHz to 42 MHz
- Trigger inputs and signal outputs with timers

Analog Signal Path

- 75 Ohm $\pm 2\%$ input impedance on selected channel, 77 Ohm $\pm 2\%$ on non-selected channels
- Frequency response:
 - 0–10 MHz: ± 1 Db
 - 0–20 MHz: $\pm 1-2$ Db
 - 0–40 MHz: $\pm 1-3$ Db
- Low frequency cutoff with AC coupling: 5 Hz (max)
- Clamp droop rate:
 - DC coupling: 1 LSB/msec. (maximum)
 - AC coupling: 10 LSB/msec. (maximum)
- Clamp acquisition rate: 20 LSBs/mS (minimum)

- DC restore clamp pulse can be 4 μ S for RS-170/CCIR derived from incoming composite video back porch or an internally generated programmable H timing signal with 1 pixel timing resolution, or disabled (DC coupling)
- Clamp and coupling controls are common to both channels
- Programmable gain over a range of 0.5–2.0 in 150 1% steps to accommodate input signals ranging from 0.5–2.0 V
- Programmable offset in DC coupling mode, accepts ± 4.0 V input; control has approximately 200 steps over that range
- Programmable DC clamp level with 200 steps over range of -72 to $+328$ (400) ADC units; each step is 2.0 LSBs nominal
- Gain, offset, and clamp are factory calibrated with offsets in EEPROM; software controls the use of offset calibration
- Sync separator works with RS-170, CCIR, RS-343 sources; accepts negative-going sync levels between 0.15 and 0.60 V

Physical Specifications

Height: 0.56 inches (14 mm)
 Length: 3.3 inches (84 mm)
 Width: 2.1 inches (53 mm)
 Weight: 1.4 ounces (39.7 grams)

Power Requirements (all voltages are $\pm 5\%$)

+5 Volts 70 mA (typical)
 +12 Volts 250 mA (typical)
 -12 Volts 140 mA (typical)
 5.03 Watts total (typical)

Environmental Specifications

Operating Temperature: 0° to 55° C
 (32° to 131° F)
 Maximum Chip Case Temp: 85° C
 (185° F)
 Storage Temperature: -40° to 100° C
 (-40° to 212° F)
 Relative Humidity: 10% to 90%
 (non-condensing)
 Air Flow Requirement: 50 LFPM (min)

Additional Information

For related product information, refer to the following Datacube literature:

[MaxPCI Data Sheet](#)
[MaxACQ Architecture Data Sheet](#)
[DatacubeWIT Data Sheet](#)
[PC ImageFlow Data Sheet](#)

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