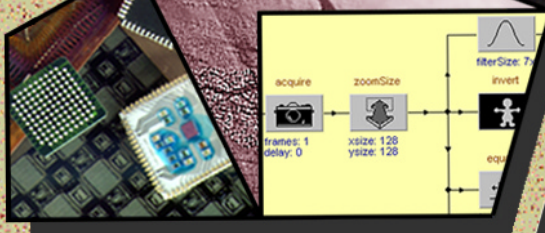


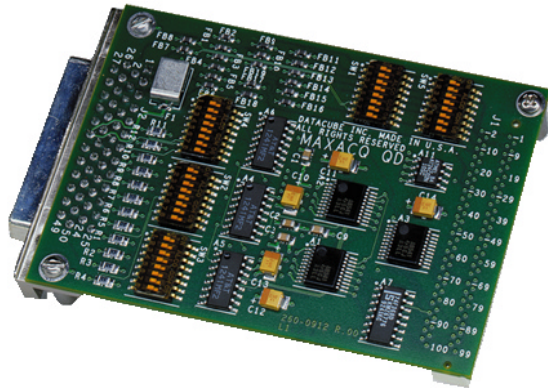


Vision By
MaxPCI®



QD MaxACQ Module

42 MHz Digital TTL Acquisition



- Interfaces to a wide variety of one- and two-dimensional cameras and sensors
- 16-bit single-ended digital image acquisition at 42 MHz
- 42 MHz 16-bit FIFO capable of holding up to 300 K pixels
- Highly efficient and noise-isolated MaxACQ architecture

MaxACQ Architecture

The QD module is one of the MaxACQ family of acquisition daughter-cards from Datacube.

The MaxACQ modules provide high throughput and simplify integration for a variety of cameras or sensors including area, line-scan, and TDI types, in a range of resolutions.

Under the MaxACQ architecture, those functions such as timing control that are required by all types of acquisition (analog, digital, color, etc.) are handled by the image processing motherboard. This division of responsibilities results in individual acquisition modules that are smaller and less costly, with reduced noise.

Each of the MaxACQ modules uses a fine-pitch SCSI-style connector for easy integration. The use of an industry-standard connector cuts the cost and effort associated with building custom cables. Many of the required cables are available off-the-shelf, making the modules in the MaxACQ family more easily interchangeable.

Digital Acquisition

The QD acquisition module provides digital image acquisition for all boards that use the MaxACQ architecture. The QD module supports a wide variety of one- and two-dimensional digital cameras and sensors. It accepts 16-bit single-ended or 12-bit differential digital data inputs at up to 42 MHz. Flexible receivers allow the QD module to accept a wide variety of differential and single-ended data schemes, including TTL, CMOS, RS-422, PECL logic, and LVDS signals.

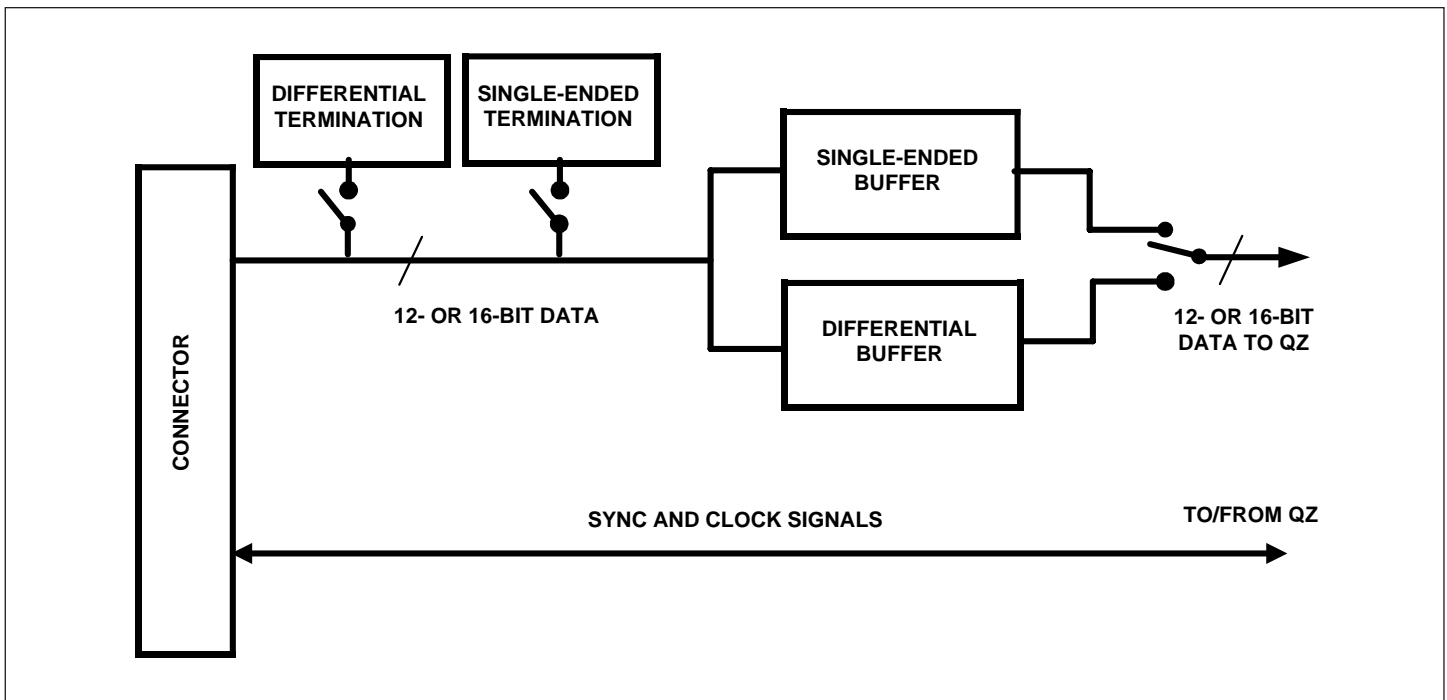
Features

- Interfaces to a wide variety of one- and two-dimensional cameras and sensors
- 42 MHz acquisition rates
 - 12-bit acquisition in differential mode
 - 16-bit acquisition in single-ended mode
- EEPROM for ID and revision data

Specifications

Digital Inputs

- Accepts 16-bit single-ended or 12-bit differential digital inputs, operating at 42 MHz
- 16-bit single-ended data:
 - Input levels are TTL compatible
 - Schmidt trigger receivers with hysteresis improve noise immunity



Block Diagram of the QD MaxACQ Module

- 12-bit differential data:
 - Input receivers are differential RS-422 types
 - Performance similar to standard RS-422
 - Inputs have hysteresis for improved noise immunity
 - Functions well in long cable drive (up to 20 meters) applications
 - Compatible with LVDS and PECL standard signals
- EEPROM support for ID and revision data

Timing

- Sensor interface with differential or single-ended inputs
- Flexible sync selection
- ADC clock can be provided externally or internally:
 - External clock coming from scanner or cameras from DC to 42 MHz
 - Arbitrary (internal) clock can be synthesized from 15 KHz to 42 MHz

Input Data Buffer

- 42 MHz, 16-bit FIFO, capable of holding up to 300 K pixels, allows seamless processing of images in line-scan applications (continuous vertical)

Physical Specifications

Height: 0.56 inches (14 mm)
 Length: 3.3 inches (84 mm)
 Width: 2.1 inches (53 mm)
 Weight: 1.1 ounces (31.2 grams)

Power Requirements (all voltages are $\pm 5\%$)

+5 Volts 600 mA (typical)
 3.00 Watts Total (typical)

Environmental Specifications

Operating Temperature: 0° to 55° C
 (32° to 131° F)
 Maximum Chip Case Temp: 85° C
 (185° F)
 Storage Temperature: -40° to 100° C
 (-40° to 212° F)
 Relative Humidity: 10% to 90%
 (non-condensing)
 Air Flow Requirement: 50 LFPM (min)

Additional Information

See the QD module block diagram above. For related product information, refer to the following Datacube literature:

[MaxPCI Data Sheet](#)
[MaxACQ Architecture Data Sheet](#)
[DatacubeWIT Data Sheet](#)
[PC ImageFlow Data Sheet](#)

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