Vision By MaxPCI®

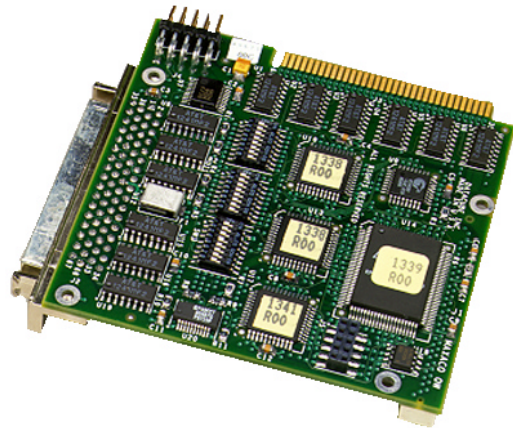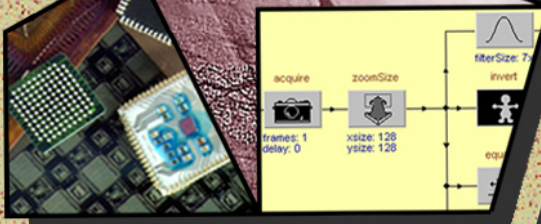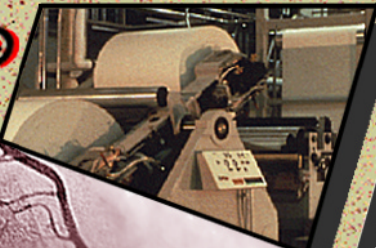# QW MaxACQ Module
Wide Differential Digital Acquisition

High Bandwidth, Flexible Differential Data Acquisition

- 8-, 12-, 16-, 24-, and 32-bit digital image acquisition at up to 120 MB/second

- RS-422, LVDS (RS-644), and PECL differential digital data acquisition

- 68-pin SCSI style input connector is compatible with AIA digital sensor specification

- Acquire from up to four 8-bit sensors simultaneously with separate H and V clocks

- Highly efficient and noise isolated MaxACQ architecture

- Supports long cable lengths from sensors

QW MaxACQ Module

The QW MaxACQ module provides flexible wide-bandwidth differential digital image acquisition for MaxPCI and other boards that use the MaxACQ architecture.

The challenge with interfacing to multiple digital cameras is that they can not be synchronously locked together with the necessary degree of precision. Digital area cameras can only be locked vertically, their pixel clocks can not be locked. Their respective clocks will drift between cameras due to differing cable lengths and characteristics, and temperature variations of the cameras themselves. On the other hand, line scan cameras can only be locked horizontally.

MaxACQ QW solves these problems by providing the necessary timing interfaces required to lock together up to four 8-bit 20 MHz cameras, two 8-bit dual-tap 20 MHz cameras, one 8-bit quad-tap 20 MHz camera, two 8-bit 40 MHz cameras, or one 8-bit dual-tap 40 MHz camera.

The QW module supports a wide variety of one- and two-dimensional digital cameras and sensors. The QW module specializes in the acquisition of a variety of differential signal types including RS-422, LVDS (RS-644), and PECL logic.

It acquires one or more 8-, 12-, 16-, 24-, or 32-bit data signals, at bandwidths up to 120 MB per second.

Many popular sensors which support the AIA digital input standard can be connected directly to the QW using off-the-shelf cables. This standard, which uses 68-pin fine-pitch SCSI-style connectors, allows readily available industry-standard cables to be used. This minimizes integration cost and effort by eliminating the need to build custom cables.

Easy to Use

Datacube's Camera Interface File (CIF) technology allows you to use QW with virtually no programming effort. CIFs for popular sensors are available. A point and click tool to build your own CIFs is also available. Simply reference the CIF file for your sensor in your PC ImageFlow, DatacubeWiT, or MaxLab environment and begin acquiring differential digital data right away.

MaxACQ Architecture

The MaxACQ family of acquisition modules supports a broad range of analog and digital cameras and sensors including area, line-scan, and TDI. The family includes easy to integrate solutions for applications requiring a wide range of acquisition throughputs and resolutions.

This architecture provides for more reliable operation, because noise sensiitve components on the acquisition modules are isolated from noise generating circuitry (e.g clock generation and phase-lock loop) implemented on the motherboard.

The MaxACQ architecture also allows the individual acquisition modules to be smaller, and less costly.

Features and Specifications

Cameras and Sensors

- Supports sensors with differential RS-422, LVDS (RS-644), and PECL outputs
- Interfaces to a wide variety of one- and two-dimensional differential cameras and sensors
- Utilizes the AIA digital input 68-pin, fine-pitch, SCSI-style connector standard for quick and easy sensor integration

Digital Data Inputs

- 16-bit acquisition at up to 50 MHz rates
- 24-bit acquisition at up to 40 MHz rates
- 32-bit acquisition at up to 20 MHz rates
- Differential termination
  - 110 Ohm termination across each differential signal pair
  - All terminations are always enabled
- Input Line Receivers
  - Accepts RS-422, LVDS (RS-644), and PECL level signals
  - Schmidt trigger receivers with hysteresis improve noise immunity
  - Functions well in long cable applications (up to 20 meters)
- Acquisition FIFOs
  - Allows acquisition from up to four identical cameras with the same acquisition frequencies, but asynchronous Hsyncs up to +/-4096 pixels

- Requires no master clock when used with multiple cameras

Timing Interface

- Supports the use of the following MaxACQ signals for flexible sync selection:
  - Clock In/Out (differential)[1]
  - External H, V/CS In (differential)
  - Auxiliary 1 In/Out (differential)
  - Auxiliary 2 In/Out
  - H and V Out (differential)
- Clock In and Out signals can be disabled (via onboard switches) when they are not used, to reduce the generation of noise
- Sample clock can be provided externally or internally:
  - External clock coming from scanner or cameras from DC to 50 MHz
  - Arbitrary (internal) clock can be synthesized from 160 KHz to 42 MHz

Physical Specifications

Height:	0.56 inches (14 mm)
Length:	3.3 inches (84 mm)
Width:	2.1 inches (53 mm)
Weight:	1.1 ounces (31.2 grams)

Power Requirements (all voltages are ±5% and apply to revision 1 QW boards)

+5 Volts	1.00 A	(typical)
3.30 Volts	500 mA	(typical)
6.65 Watts	Total	(typical)

PCI Chassis Backpanel I/O Slots

- QW can use up to three backpanel connector plate slots depending upon I/O signal routing and data width

Environmental Specifications

Operating Temperature: 0° to 55° C (32° to 131° F)

Maximum Chip Case Temp: 85° C (185° F)

Storage Temperature: -40° to 100° C (-40° to 212° F)

Relative Humidity: 10% to 90% (non-condensing)

Air Flow Requirement: 50 LFPM

Module

- EEPROM contains device ID and manufacturing revision data which can be read using supplied utility

Additional Information

For related product information, refer to the following Datacube literature:

MaxPCI Data Sheet
MaxACQ Architecture Data Sheet
DatacubeWiT Data Sheet
PC ImageFlow Data Sheet

[1] Due to RFI and cabling issues Datacube does not recommend the use of Clock Out unless mandatory for the camera in use.

QW Acquisition Modes

Cameras	Taps/Camera	Maximum Bits/Tap	Maximum Data Rate (MHz)/Tap
1	1	32-bit	20
2	1	16-bit	20
2	2	8-bit	20
3	1	8-bit	20
4	1	8-bit	20
1	1	16-bit	40
2	1	8-bit	40
1	2	8-bit	40
1	3	8-bit	40 (with Revision 3 MaxPCI)