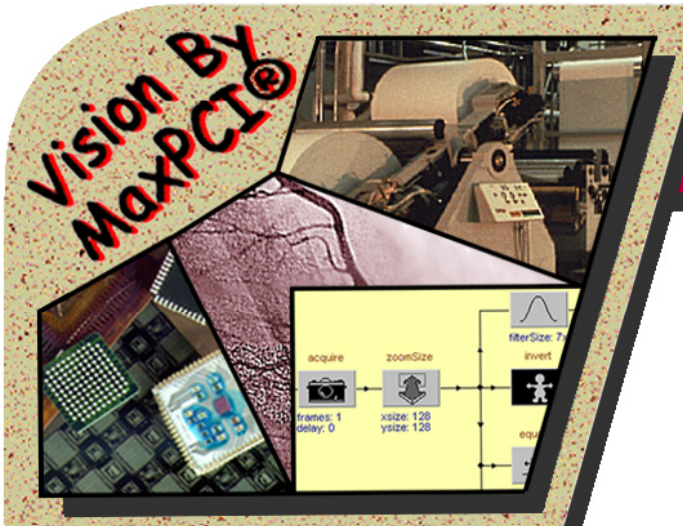
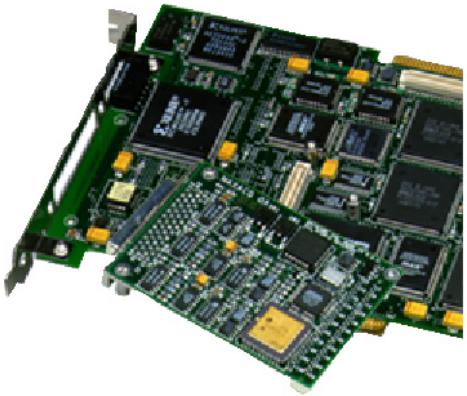
MaxACQ Architecture



High Performance Image Acquisition for Datacube Products

- Supports nearly all line scan and area cameras and sensors including multiple sensors, multiband and multitap varieties
- ImageFlow and PC ImageFlow provide a powerful, consistent sensor programming interface across all Datacube products
- Easily integrated into real world image processing & machine vision systems
- Flexible, modular design uses MaxACQ modules to address sensor specific requirements



Datacube's modular architecture for image acquisition is called MaxACQ. This architecture consists of a variety of sensor-dependent MaxACQ modules which plug into the QZ device, a part of the motherboard circuitry on all MaxACQ-compatible hardware products. The MaxACQ architecture is in use today on Datacube's MaxPCI and *mvPower* image processors.

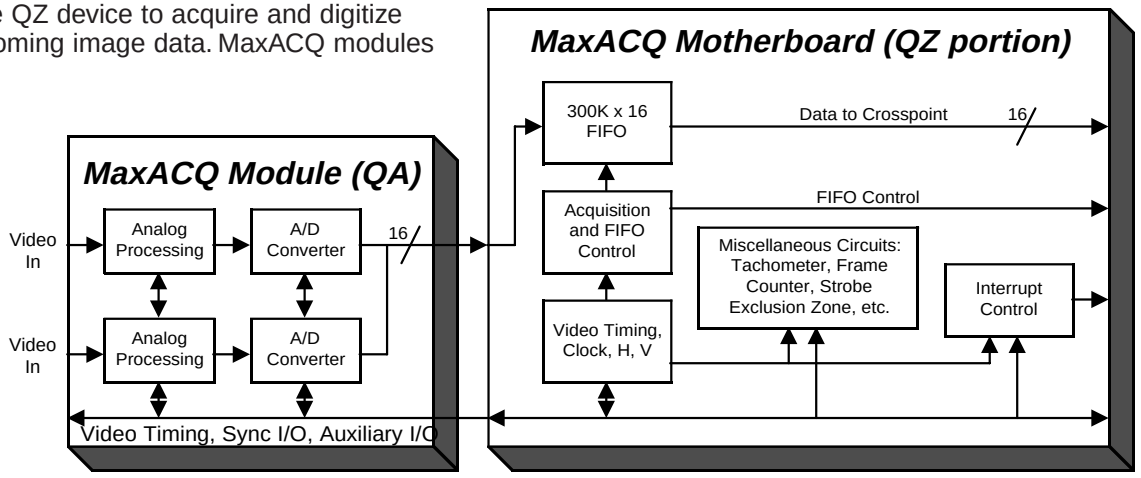
The QZ device performs image acquisition tasks that are common to all sensors. It contains a powerful FIFO controller and programmable timing generator, and can provide sensor clock generation using phase locking, clock synthesis, or clock slaving. It also contains various acquisition support functions to simplify interfacing to various strobed and asynchronous sensors, continuous web systems, and other sensor peripherals.

Specialized front-end MaxACQ modules (for example, QA for analog acquisition and QD for digital acquisition) plug onto the image processing motherboard and work with the QZ device to acquire and digitize incoming image data. MaxACQ modules are now available to handle most acquisition needs. Other modules in development will allow MaxACQ users to interface to virtually all cameras and sensors available today. The simplified block diagram (below) illustrates how QZ works with MaxACQ modules to address acquisition needs.

QZ's capabilities allow up to 16Kx16K sensors operating at up to 80 MB/sec. via two 8-bit wide 40 MHz data paths. QZ's two 8-bit, 300K long FIFOs allow very flexible acquisition timing including continuous vertical (web) applications.

Features

- Up to 42 MHz acquisition/transfer of 16-bit data
- Programmable timing model similar to Datacube's AS, AD, and older MAX-SCAN acquisition devices
- Common ImageFlow software interface (Datacube's Video Object) across all products
- Common cabling across similar products
- Line length to 16K pixels
- Frame length to 16K lines
- MaxACQ modules use EEPROM for identification, factory configuration, and calibration



- Able to generate regular FIFO control timing for a wide range of sensors. Regular FIFO control timing allows sensor data to be directly processed through elements with vertical scope such as convolvers.
- Programmable sync processor
  - Handles video with equalization and serration pulses
  - Provides stable sync separation from composite video and composite sync signals
- Easy support for continuous V using a single VSIM
- Line and frame counters, free running, with input capture for storing line or frame count upon an event
- Tachometer to measure sensor H rate
- Direct external fire command synchronization
- Control for implementing a strobe exclusion zone
- Four interrupts including two external sources

Specifications

Acquisition Clock Specifications

- Clock can be phase locked, generated from an arbitrary synthesizer, or received from an external source
- In phase lock, clock ranges from 5.0 to 42.0 MHz
- H input to Phase Lock Loop ranges from 15 to 100 KHz
- In clock synthesizer mode, clock ranges from 165 KHz to 42 MHz

Acquisition Horizontal Timing Specifications

- 16,383 long horizontal counter and pulse decoders operate at up to 42 MHz
- Programmable, single-pixel precision control of all signals
- Generates:
  - HSYNC – Timing to sensor
  - HACTIVE – Controls acquisition timing
  - HPERIOD – Controls period of H in master mode
  - HAUX1 and HAUX2 – auxiliary output signals
- Horizontal timing can be synchronized to an external H or composite sync, or composite video (on analog modules) using either phase locking or resetting of the H counter.
- HSYNC to active minimum: 0 pixels
- HBLANK min: 8 pixels
- HSYNC width minimum:
  - With HSYNC processor used to remove equalization pulses: 200 ns
  - Otherwise: 25 ns
- HSYNC processor detects the horizontal sync from composite sync

Acquisition Vertical Timing Specifications

- 16,383 long vertical counter and pulse decoders operate at up to 42 MHz
- Programmable, single-line precision control of all signals
- Generates:
  - VSYNC – Timing to sensor
  - VACTIVE – Controls acquisition timing
  - VPERIOD – Controls period of V in master mode
  - VAUX1 and VAUX2 – auxiliary output signals
- External V, vertical reset, CPU controlled or internal timing
- VBLANK minimum: 2 lines
- VSYNC to active minimum:
  - Interlaced: 1 line
  - Non-interlaced: 0 lines
- Interlaced and progressive scan (non-interlaced) operating modes
- Asynchronous external triggered acquisition
- Continuous vertical acquisition for use with line-scan cameras
- VSYNC processor detects the vertical sync from composite sync

Additional Sensor Support Functions

- Auxiliary inputs (used to generate interrupts or control miscellaneous circuits):
  - AUXIN1 – differential input
  - AUXIN2 – single-ended input
- Auxiliary outputs:
  - AUXOUT1 – differential output
  - AUXOUT2, AUXOUT3 – single-ended outputs
- QZ logic generates four active-high interrupts. Select logic determines the sources for the interrupts:
  - VAUX1 or VAUX2: Any line in a frame
  - VACTIVE or /VACTIVE: Beginning or end of vertical active
  - STROBE: External strobe signal
  - HSYNC: Every H line
  - VSYNC or /VSYNC: Beginning or end of vertical sync out
  - AUXIN2 or /AUXIN2: Rising or falling edge of AUXIN2
  - Synchronization Error
  - FIFO Transfer Done
- Tachometer: 16 bits, updated every 1.64 ms with selectable input

Signal Levels and Terminations

- MaxACQ's timing and control signal receivers support the following signal types:
  - Single-ended positive going TTL or CMOS, 1.4V threshold
  - Single-ended negative going TTL or CMOS, 1.4V threshold
  - Single-ended open collector drivers, if termination is used
  - Terminated or unterminated inputs
  - Termination in 110 ohms to 2.85 V under software control
  - Termination with 110 ohms differential on digital MaxACQ modules
  - Differential RS-422 up to 20 MHz
  - Differential PECL up to 42 MHz
  - Differential LVDS (RS-644) up to 42 MHz
- MaxACQ module 110-ohm differential termination is required for PECL and LVDS (RS-644), recommended for RS-422
- Single-ended inputs are TTL/CMOS compatible
- Differential inputs use high speed receivers:
  - 200 mv input sensitivity with hysteresis
  - Common mode range >0.0 and <5.0V
  - Static protected
  - TTL, CMOS, RS-422, PECL, and LVDS (RS-644) compatible
- Differential outputs are nominally RS-422 levels; able to drive:
  - Single-ended positive going TTL inputs
  - RS-422 inputs
  - PECL inputs
  - 110-ohm terminations (recommended for RS-422 and PECL inputs)
  - Single-ended outputs are nominally TTL levels

FIFO Control Logic

- QZ is always a pipe timing master
- Rules for regular timing:
  - No restrictions on surface size
  - Must have a predictable horizontal frequency
- QZ FIFO control bus:
  - Single-shot or continuous mode
  - Externally triggered FIFO transfers
  - Software selectable FIFO transfer type (framing mode)
- Control software manages the acquisition FIFO, ensuring that it never completely empties or overflows

Switching Characteristics

		QD Module		QA Module	
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**
T_{DSU}	Data set-up time to clock in	4 ns	----	Not Applicable	
T_{DH}	Data hold time to clock in	----	6 ns	Not Applicable	
T_{HINSU}	HSync setup time to clock in	4 ns	----	4 ns	----
T_{HINH}	HSync hold time to clock in	----	4 ns	----	4 ns
T_{CKH}, T_{CKL}	Clock width minimum	11 ns	----	11 ns	----
$T_{HOUT(Ck-Q)}$	Clock in to HSync out	----	26 ns	----	26 ns
T_{CK}	Clock period	23.8 ns	----	23.8 ns	----

QZ to MaxACQ Module, 100-pin Connector Signals

- General purpose interface control bus
- Two 8-bit data paths operating at up to 42 MHz for sensor data
- Motherboard-supplied power supply voltages:
  - +3.3 V
  - +5.0 V
  - +12.0 V
  - -12.0 V
- QZ generated sensor timing and data signals, including all differential inputs and outputs, such as syncs, clocks, auxiliary inputs and outputs.
- I^2C Bus used for EEPROM and control: MaxACQ module identification, calibration data, etc.

QZ Acquisition Bandwidth

The MaxACQ architecture's *sensor data rate* is defined as the maximum rate at which QZ can accept data from a sensor or camera. It can be calculated by multiplying the number of pixels in a line of the incoming image by the sensor line rate measured in Hz. In general, the QZ sensor data rate is limited by the bandwidth of the motherboard's AM memory device (VSIM). It is a function of both the horizontal surface (H) size, and whether or not the AM transmit and CPU access ports are used simultaneously with a receive transfer from QZ.

The following tables show blanking requirements of VSIM (AM) as a function of gateway use, CPU access, and line length. Both receive and transmit functions use the same blanking numbers or percentages.

The following recommendations apply to all pipes involving QZ and the AM device:

- If both receive and transmit gateways are active at 40 MHz, limit line lengths to 3584 pixels.
- If line lengths greater than 3584 must be used and the sensor data rate is less than 20 MHz, set the AM receive gateway and the QZ to 20 MHz.
- If line lengths are greater than 3584 and sensor data rate is greater than 20 MHz, use double buffering. This will allow one AM to receive while the other transmits, after which they swap roles.
- If both gateways are operating at 40 MHz simultaneously, do not allow CPU access on that gateway.

Additional Information

See the last page of this data sheet for a simplified timing diagram of the QZ device. For related product information, refer to the following Datacube literature:

MaxACQ Data Sheets
MaxPCI Data Sheet
DQWiT Data Sheet
PC ImageFlow Data Sheet

Into AM Receive @ 40 MHz, no CPU access

Conditions	Blanking req.	Net Data Rate	Size (H)
Transmit Gateway Idle	4 pixels	39.9 MHz	16000 Max
Transmit Gateway 20 MHz	4 pixels	39.9 MHz	16000 Max
Transmit Gateway 40 MHz	10%	36.0 MHz	3584 Max

Into AM Receive @ 40 MHz, CPU access

Conditions	Blanking req.	Net Data Rate	Size (H)
Transmit Gateway Idle	4 pixels	39.9 MHz	16000 Max
Transmit Gateway 20 MHz	4 pixels	39.9 MHz	16000 Max
Transmit Gateway 40 MHz	38%	24.8 MHz	1024 Max
Transmit Gateway 40 MHz	---- Not Recommended ----		<1024

Into AM Receive @ 20 MHz, with or without CPU access

Conditions	Blanking req.	Net Data Rate	Size (H)
Transmit Gateway Idle	4 pixels	19.9 MHz	16000 Max
Transmit Gateway 20 MHz	4 pixels	19.9 MHz	16000 Max
Transmit Gateway 40 MHz	4 pixels	19.9 MHz	16000 Max

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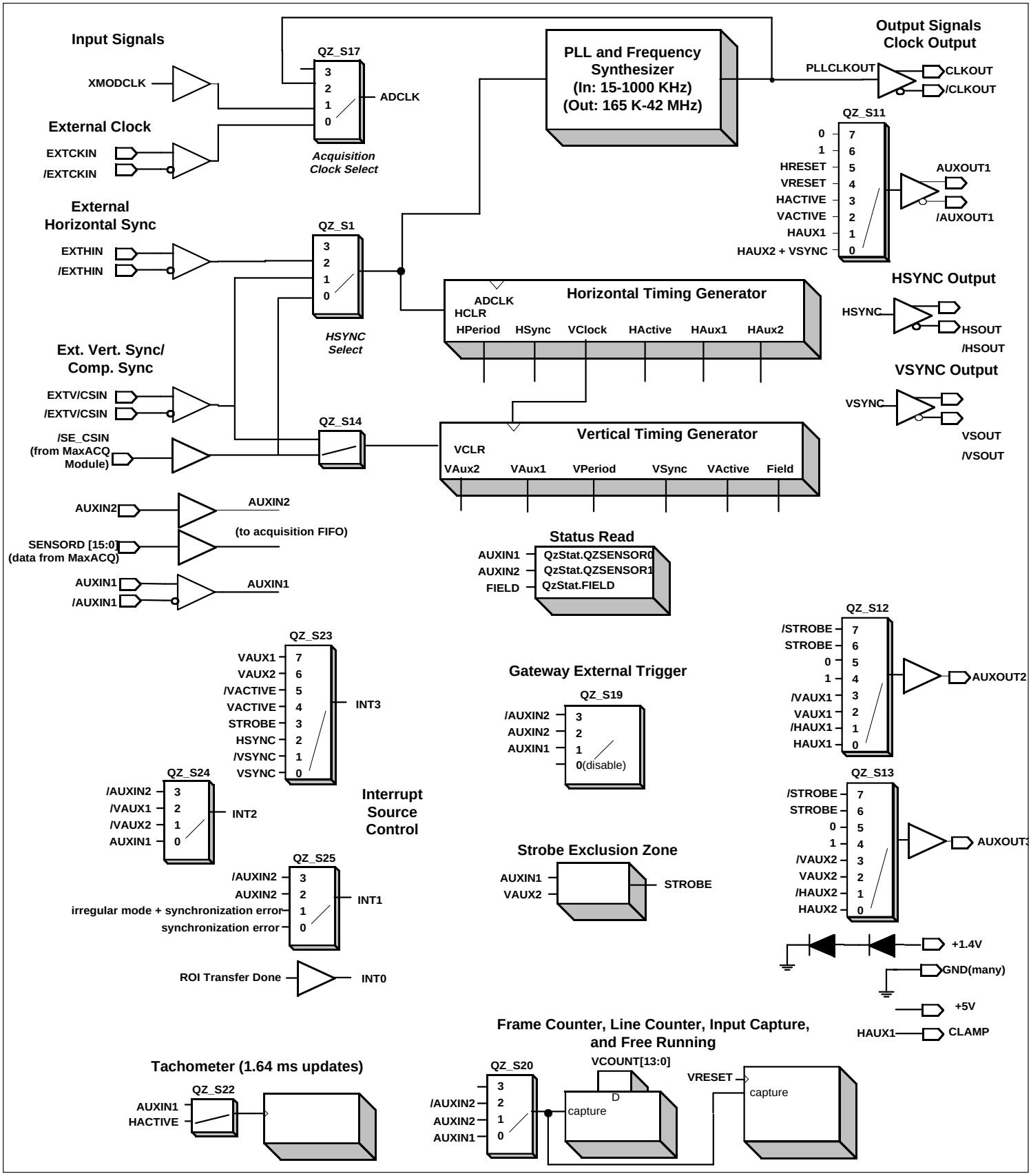

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